WP 3: Data processing, evaluation and visualization

WP coordination: UCA

Task 3.1: Framework for parallel computation

Contributors: IPE, UCA, SCI

The programmability of the data processing module is eased by the use of a higher-level software framework, increasing the productivity of programmers. The goal is to develop a stack of software tools which allow rapid development and deployment of a large range of parallel data processing algorithms. We propose the three layer structure: The first layer implements the core part of the stack which is a set of API's which would automate exploitation of the developed infrastructure. This shall include the data readout from the fast data link to the camera, transportation to the graphic card, decompression, display of results, and finally the feedback control of the camera. The next layer is a collection of parallel primitives for image processing and numerical computation using FPGAs and GPUs as co-processors. The top level of the framework should structure the development process. A task scheduler should distribute the computation tasks between available co-processors. The developer is expected to provide only the processing, visualization, and control plugins while everything else is automated by the framework.

For the specification of the requirements and the definition of the interfaces workshops between the contributing partners are foreseen. In general the framework should base open source packages. The main supported operating system will be Linux.

Deliverables:

a) GPU computing platform
b) Framework with the three layers:
    - Infrastructure functions for hardware management
    - Standard image processing functions
    - Task scheduler, load balancing
c) Example programs
d) Documentation

Milestones:

a) Investigation of expected implementations and specification of the requirements to the framework (month 2)
b) Assembly of GPU Computing Platform (month 3)
c) Definition of standard interfaces and naming conventions, selection of parallel programming languages (month 8)
d) Development of infrastructural part of the framework (month 14)
e) Selection, development, optimization and characterization of standard functions for image processing (month 26)
f) Development of the top level framework (month 32)

Task 3.2: Development of data processing and assessment algorithms for streamed data on parallel hardware

Contributors: UCA, IEKP, TPU
(supported for algorithm development by: SCI, LAS, ISS)

Data evaluation algorithms can benefit from the vast amounts of computational power provided by high-performance graphics adapters and FPGAs. Data evaluation algorithms should be developed which use this computational power, reducing the computation time from hours to minutes or even seconds for a given evaluation algorithm.

In pre-studies to this project, tomographic and laminographic reconstruction time was reduced by two orders of magnitude using GPUs as compute co-processor. Based on the framework developed in task 3.1, parallel algorithms for the processing of projection data will be implemented. In a second step the existing algorithms need to be optimized with respect to the high-speed, high throughput setup developed in WP2. In order to preserve a good image quality while increasing the frame rates, algorithms need to be developed to automatically monitor the complete data chain from the mechanics and detector to the processing. This is also the basis for the control tasks in WP4.

Deliverables:

a) Laminographic and tomographic reconstruction library for multiple GPUs
b) Example programs to illustrate the usage of the library
c) GPU-enabled reconstruction software for processing of streams of projection data
d) Algorithms for data assessment in a high-speed, high-throughput setup
e) Documentation

Milestones:

a) Port of existing processing algorithms to parallel framework, setup of library with parallel executable code. (month 20)
b) Reconstruction applications ported to parallel library for processing of streams of projection data (month 26)
c) Optimized algorithms for high-speed, high throughput setup, extension of the parallel code library. (month 32)

Task 3.3: Graphical user interfaces and visualization of datasets

Contributors: UCA, TPU

To ease the use of the integrated data processing and detector system, graphical user interfaces will be developed which are easy to learn and to use. This is important for development and commissioning of the automatic control features and will be beneficial to future external users, which only have a limited amount of time to conduct their experiments.

Commercially available visualization tools are, in general, not only capable of visualizing data, but offer a plethora of other functionalities, making them hard to learn and to use. The goal is to develop a software package that is specialized in only visualizing scientific datasets, reducing the complexity of the tool.

Deliverables:

a) Graphical user interface to adjust camera parameters
b) Graphical user interface to adjust control loop parameters
c) Software package including graphical user interface and programming library for visualization of scientific datasets
d) Documentation

Milestones:

a) Selection of graphical user interface framework and programming languages (month 2)
b) Functional prototypes of deliverable software (month 6)
c) Production quality version of deliverable packages (month 16).

WP 4: Development of on-line process control

WP coordination: IEKP

Task 4.1: On-line data compression and fast reject

Contributors: IPE, IEKP, ISS

A sample experiment will be selected to develop a set of algorithms and demonstrate the benefits of on-camera data compression and preprocessing using reprogrammable logic. Different lossless data compression algorithms will be investigated. A fast reject option of a given frame will be developed.

Deliverables:

a) Implementation and source code of fast frame reject
b) Implementation and source code of compression and corresponding decompression algorithms
c) Documentation

Milestones:

a) Selection of sample experiment (month 1)
b) Analysis of image characteristics (month 3)
c) Development/selection of data compression, preprocessing and fast reject algorithms (month 21)
d) Firmware development and characterization using FPGA (month 27).

Task 4.2: Development of control algorithms and feedback loops

Contributors: TPU, IEKP, ISS

Having high performance data evaluation tools available allows changing relevant experimental parameters automatically. The aim is to develop suitable control algorithms which use the results of the data analysis and evaluation stage to automate sample adjustment and change experimental conditions autonomously.

Two stages of control are foreseen: The first one based on the simple pattern recognition in the camera-side FPGA-based pre-processing, the second utilizing the complex GPU platform for any kind of sophisticated computer vision control algorithm.

Deliverables:

a) Universal control toolbox.
b) Application to demonstrator experiments.

Milestones:

a) Selection of demonstrator application (month 3)
b) Tool box with standard FPGA-based control functions (month 15)
c) Tool box with standard GPU-enabled control functions (month 15)
d) Integration and commissioning of demonstrator control (month 20)