Getting Started with the Xilinx Virtex-6 FPGA ML605 Evaluation Kit

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/24/09	1.0	Xilinx Preliminary Release.
11/18/09	1.1	Xilinx Initial Release.
12/08/09	1.1.1	Initial Release to the Web.
12/23/09	1.2	• Added “Getting Started with the Base Reference Design.” • Updated Figure 1-1, page 10, Figure 1-2, page 10, and Figure 1-20, page 23. • Miscellaneous typographical edits.
01/22/10	1.2.1	• Minor typographical edit.
06/07/10	1.3	Revised Figure 1-22, page 24 and Figure 1-29, page 30.
11/15/10	1.4	Revised “Installing the ISE Software,” page 61 describing the use of the software voucher as part of the software registration process.

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About This Guide

This user guide introduces the Virtex®-6 FPGA ML605 board features, provides instructions for setting up the hardware, and includes step-by-step procedures for verifying the ML605 board functionality.

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/support/documentation/virtex-6.htm.

- Virtex-6 Family Overview

  The features and product selection of the Virtex-6 family are outlined in this overview.

- Virtex-6 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-6 family.

- Virtex-6 FPGA Packaging and Pinout Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

- Virtex-6 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, boundary-scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-6 FPGA Clocking Resources User Guide

  This guide describes the clocking resources available in all Virtex-6 devices, including the MMCM and PLLs.

- Virtex-6 FPGA Memory Resources User Guide

  The functionality of the block RAM and FIFO are described in this user guide.

- Virtex-6 FPGA SelectIO Resources User Guide

  This guide describes the SelectIO™ resources available in all Virtex-6 devices.

- Virtex-6 FPGA GTX Transceivers User Guide

  This guide describes the GTX transceivers available in all Virtex-6 FPGAs except the XC6VLX760.

- Virtex-6 FPGA Embedded Tri-Mode Ethernet MAC User Guide

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in all Virtex-6 FPGAs except the XC6VLX760.

- Virtex-6 FPGA DSP48E1 Slice User Guide

  This guide describes the architecture of the DSP48E1 slice in Virtex-6 FPGAs and provides configuration examples.

- Virtex-6 FPGA System Monitor User Guide

  The System Monitor functionality available in all Virtex-6 devices is outlined in this guide.

- Virtex-6 FPGA PCB Design Guide

  This guide provides information on PCB design for Virtex-6 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers or to create a technical support case in WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Getting Started with the Virtex-6 FPGA ML605 Evaluation Kit

Introduction

The Virtex® -6 FPGA ML605 Evaluation Kit provides a development environment for system designs that demand high-performance, serial connectivity and advanced memory interfacing. The ML605 is supported by multiple targeted reference designs and the industry-standard FPGA Mezzanine Connector (FMC) that allows scaling and customization with mezzanine cards. Integrated tools help streamline the creation of elegant solutions to complex design requirements. This document provides:

- Introduction to the board's features
- Instruction for default hardware setup
- Step-by-step procedure for verifying the board's functionality

ML605 Evaluation Kit Contents

What is Inside the Box

- Virtex-6 FPGA ML605 Evaluation Board
- Universal 12V power supply
- Two (2) USB A/Mini-B cables (used for download and debug)
- CompactFlash Card
- DVI to VGA Adapter
- Ethernet Cat5 Cable
- ISE® Design Suite DVD
  - A full-seat of Xilinx ISE® Design Suite: Logic Edition – Device-Locked to Virtex-6 LX240T FPGA
- ML605 Documentation
  - Welcome Letter
  - Hardware Setup Guide
  - Getting Started Guide

What is Available on the Web

- Product Home Page: www.xilinx.com/ml605
- Reference design user guide, tutorials, and design files
- Schematics, Gerber, and board bill of materials (BOM)
- Additional detailed documentation

Key Features

Virtex-6 FPGA

- XC6VLX240T-1FFG1156 device

Configuration

- Onboard configuration circuitry (USB to JTAG)
- 16 MB Platform Flash XL
- 32 MB Parallel (BPI) Flash
- System ACE™ CompactFlash (CF) controller

Communication and Networking

- 10/100/1000 Tri-Speed Ethernet (GMII, RGMII, SGMII, MII)
- SFP transceiver connector
- GTX port (TX/RX,) with four SMA connectors
- USB to UART Bridge
- USB host port and USB peripheral port
- PCI Express® Gen1 8-lane (x8) and Gen2 4-lane (x4)

Memory

- DDR3 SODIMM (512 MB)
- Linear BPI Flash (32 MB) (Also available for configuration)
- IIC EEPROM (8 Kb)

Clocking

- 200 MHz oscillator (differential)
- 66 MHz socketed oscillator (single-ended)
- SMA connectors for external clock (differential)
- GTX clock port with two SMA connectors

Input/Output and Expansion Ports

- 16x2 LCD character display
- DVI output
- System Monitor
- User pushbuttons (5), DIP switches (8), LEDs (13)
- User GPIO with two SMA connectors
- Two FMC expansion ports
  - ♦ High Pin Count (HPC)
    - Eight GTX transceivers
    - 160 SelectIO™ interface signals
  - ♦ Low Pin Count (LPC)
    - One GTX transceiver
    - 68 SelectIO interface signals

Power

- 12V wall adapter or ATX
- Voltage and current measurement capability of 12V, 2.5V, 1.5V, 1.2V, and 1.0V supplies

Getting Started with the Flash Demonstration

Before installing the software, you can run some of the demonstration designs that are pre-installed on the BPI Flash, Platform Flash, and CompactFlash cards on the ML605 Evaluation Board. These demonstrations provide an overview of the board features. This evaluation kit comes with a number of pre-installed demonstrations and examples, as well as additional reference designs and application notes found on the Xilinx website. The default demonstrations on the Platform Flash and CompactFlash exercise some of the board features including verifying PCI Express connectivity and testing the UART, Ethernet, DDR3, IIC, LEDs, and other commonly used embedded processing features.

Board Features

The ML605 board features are shown in Figure 1-1. The default switch and jumper settings are shown in Figure 1-2.

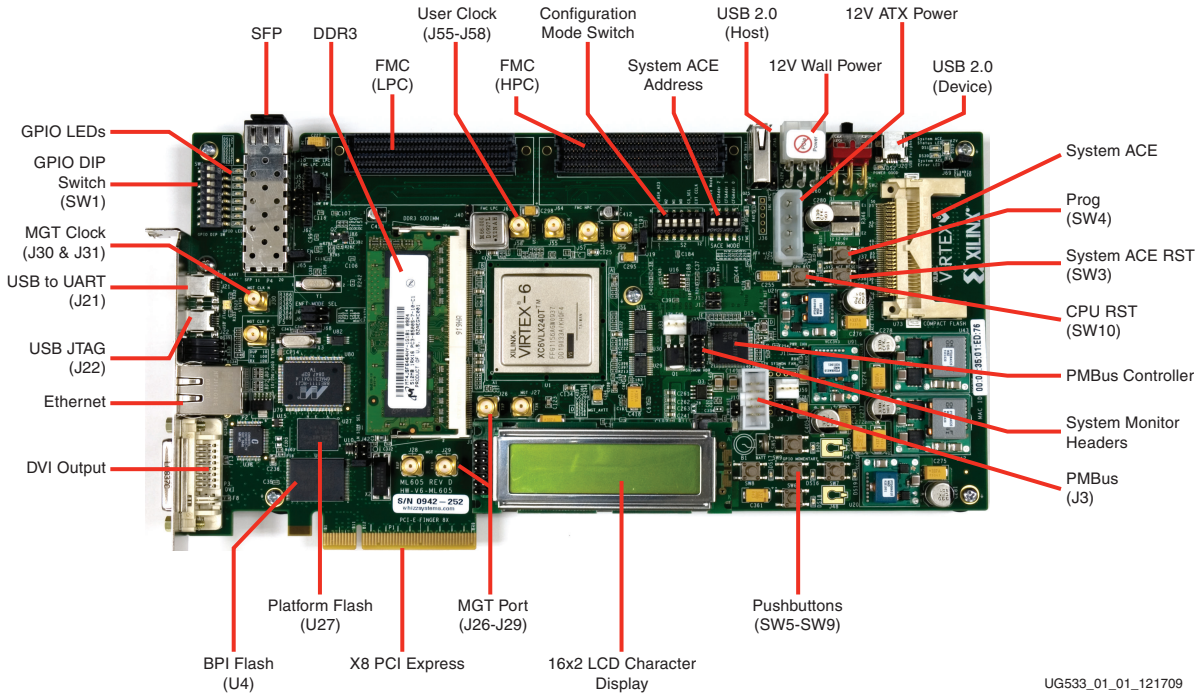


Figure 1-1: **Virtex-6 FGPA ML605 Board Features**

Ethernet GMII
J66: Shunt over 1–2
J67: Shunt over 1–2
J68: No jumper

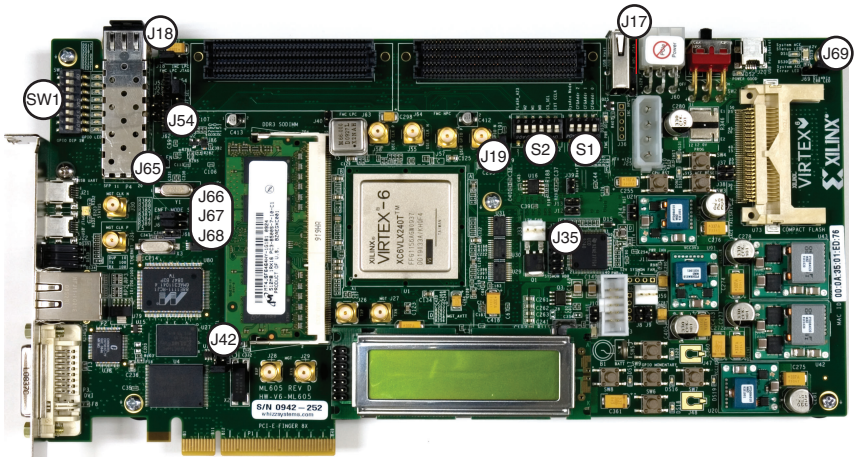
FMC Bypass
J18: Shunt over 1–2 (Bypass FMC LPC)
J17: Shunt over 1–2 (Bypass FMC HPC)
Note: *These are the JTAG chain bypasses for the FMC LPC and FMC HPC connectors.*

System Monitor
J19: Shunt over 1–2
J35: Shunt over 9–11 and shunt over 10–12

SFP
J54: Shunt over 1–2 (Full BW)
J65: Shunt over 1–2 (SFP Enable)

PCIe Lane Size Select
J42: Shunt over 1–2

System ACE CF Error LED
J69: Shunt over 1–2



S1:
4 ON (SysACE Mode = 1)
3 OFF (SysACE Addr 2 = 0)
2 OFF (SysACE Addr 1 = 0)
1 OFF (SysACE Addr 0 = 0)

S2:
6 OFF (FLASH_A23 = 0)
5 OFF (M2 = 0)
4 ON (M1 = 1)
3 OFF (M0 = 0)
2 ON (CS_SEL = 1)
1 OFF (EXT_CCLK = 0)

SW1:
8 OFF
7 OFF
6 OFF
5 OFF
4 OFF
3 OFF
2 OFF
1 OFF

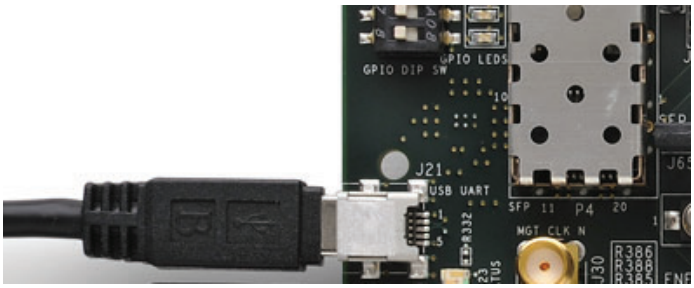
UG533_01_02_121709

Figure 1-2: **Default Jumper and Switches Settings**

Connecting the Cables and Power

The steps in this section outline how to connect the cables and power.

1. Connect one USB Type-A to mini-B 5-pin cables from your PC to J21 on the ML605 board.



UG533_01_03_061909

Figure 1-3: **Connect the Cables and Power**

2. Power on ML605 board for UART Drivers Installation
   a. Install the CP210x VCP Win2K/XP/2K3 Drivers Server from www.silabs.com.

      Note: The drivers are also available on the USB flash drive shipped with the board.

Setting the System Properties

3. Right-click **My Computer** and select **Properties**
   a. Select the Hardware tab
   b. Click on **Device Manager**

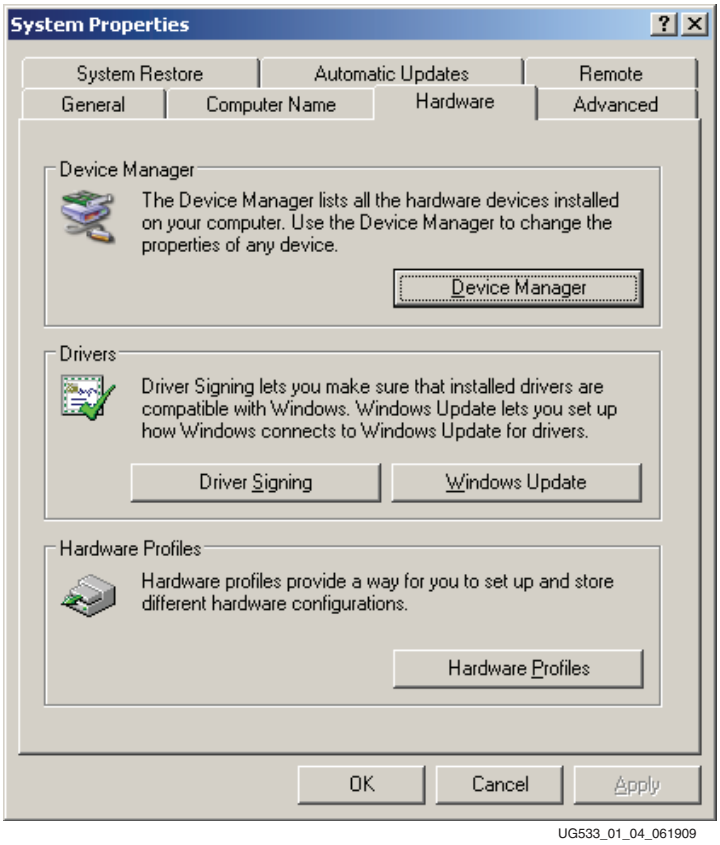


Figure 1-4: **Select the Device Manager**

4. Expand the Ports Hardware
   a. Right-click on USB to UART Bridge and select **Properties**.

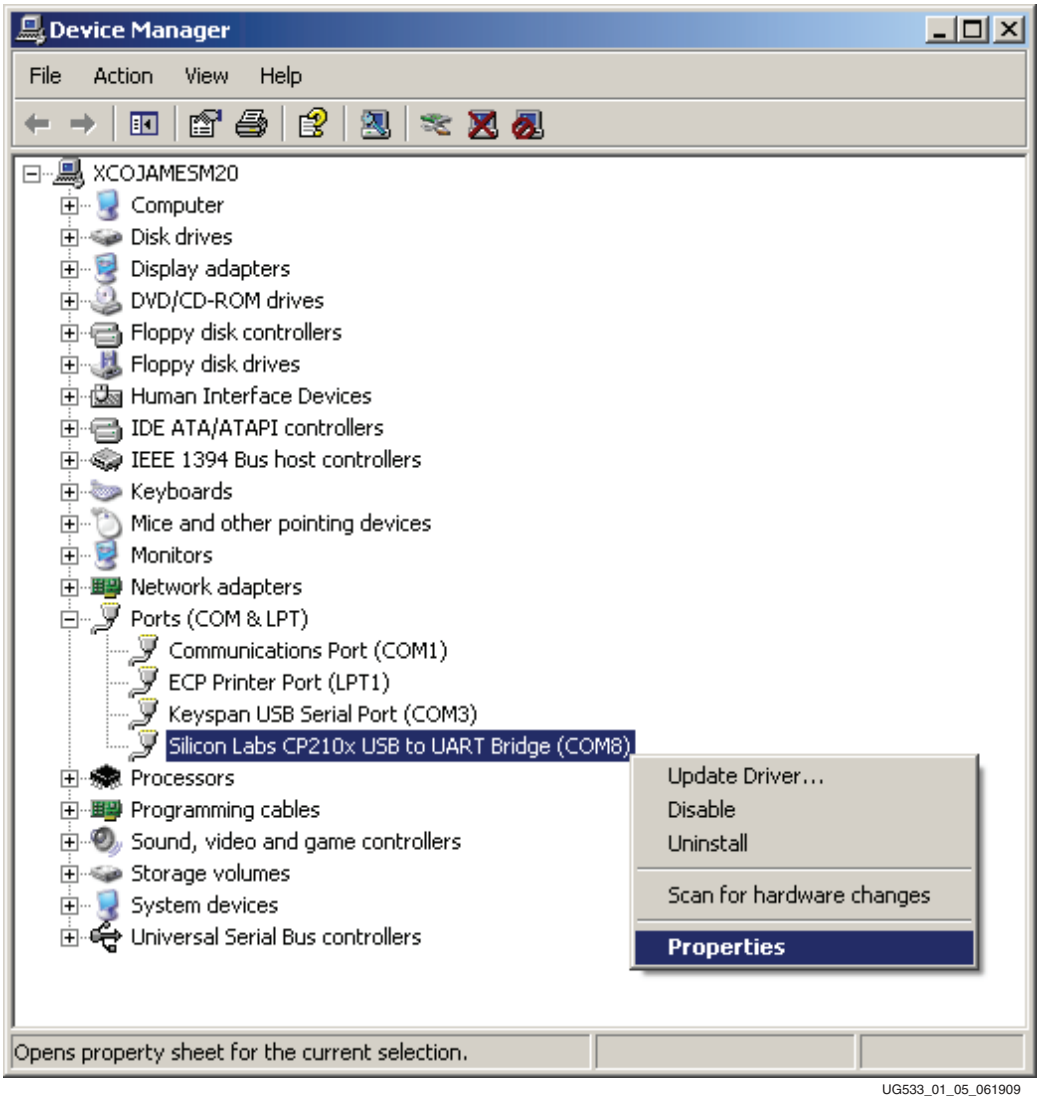


Figure 1-5: **Select the USB to UART Bridge Properties**

5. Under the Port Settings tab
   a. Click **Advanced**
   b. Set the COM Port to an open Com Port setting from COM1 to COM4.

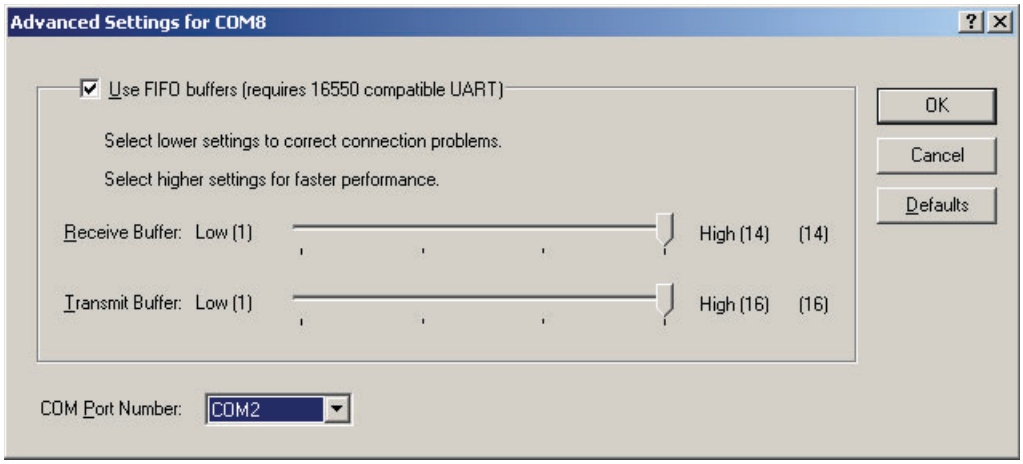


Figure 1-6: **Set the COM Port**

6. Start the Tera Terminal Program (downloadable from http://www.ayera.com/teraterm)
   a. Select your USB com port from the Port drop down window
   b. Set the baud rate to 9600

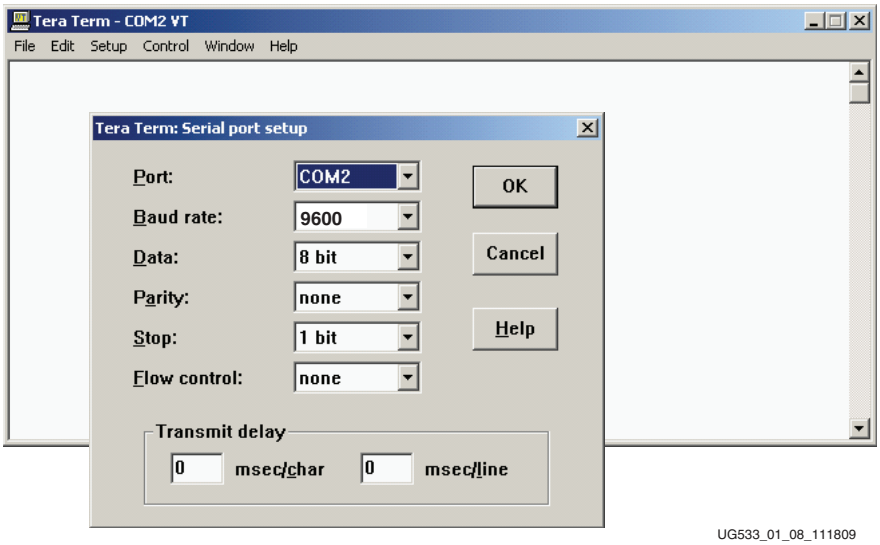


Figure 1-7: **Set the USG Com Port**

Configuring the FPGA

7. Set the DIP switch S1 to 1000 (position 4 to position 1).

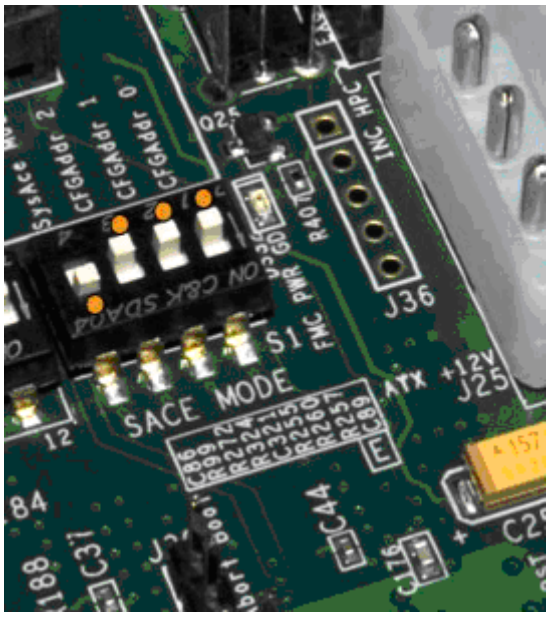


Figure 1-8: **Set the DIP Switch**

8. Insert the CompactFlash card into the card reader and press SW3, the System ACE Reset pushbutton. The CompactFlash card contains a Built-In System Test (BIST) design which is used for verification of the board's functionality.

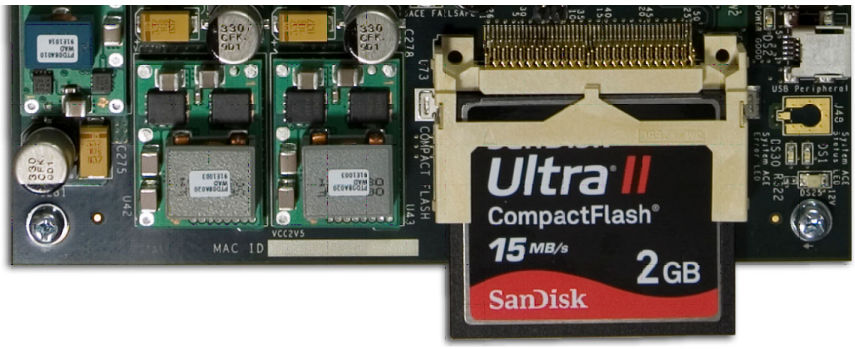


Figure 1-9: **Insert the CompactFlash Card**

9. After FPGA configuration, a menu of feature tests appears as shown in the Tera Terminal window (Figure 1-10).

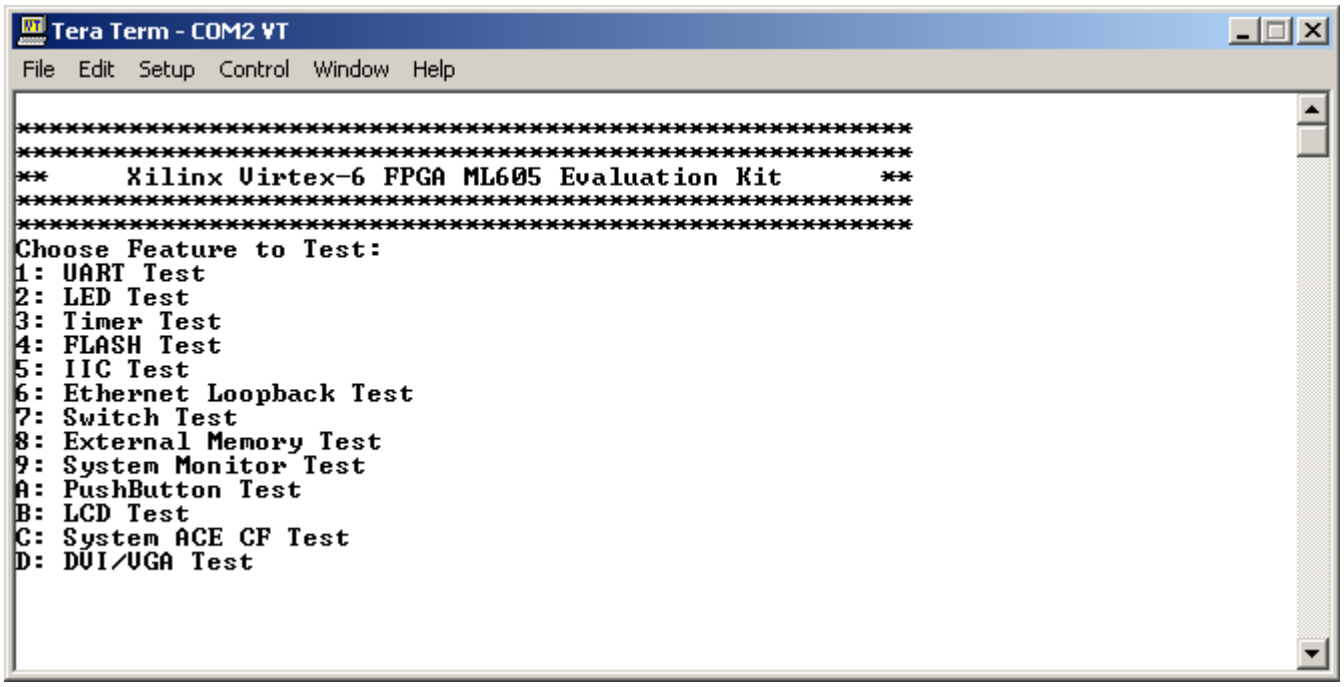


Figure 1-10: **Initial Test Menu after FPGA Configuration**

Running the BIST Application

Typing any number or character between 1 to D makes the bootloader copy the associated software application to the external DDR3 SODIMM memory and run it.

10. Type a **1** to start the UART test.

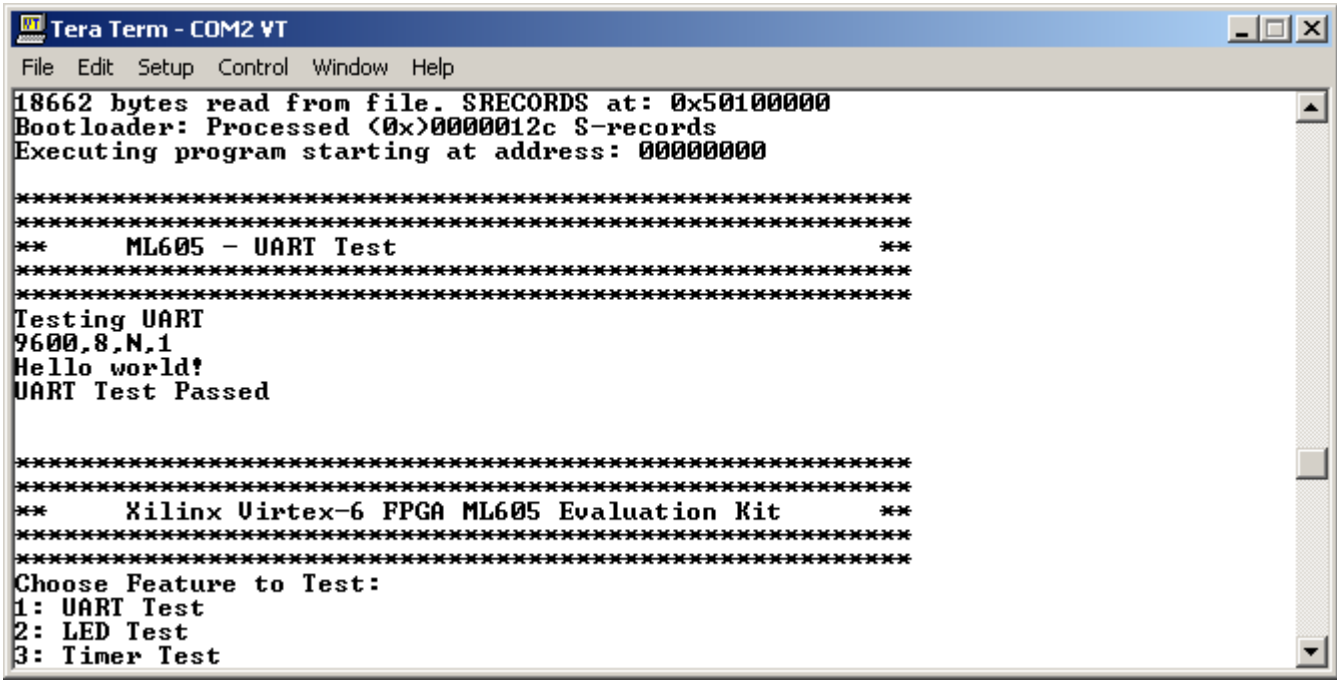


Figure 1-11: **1. UART Test**

11. Type a **2** to start the LED test.

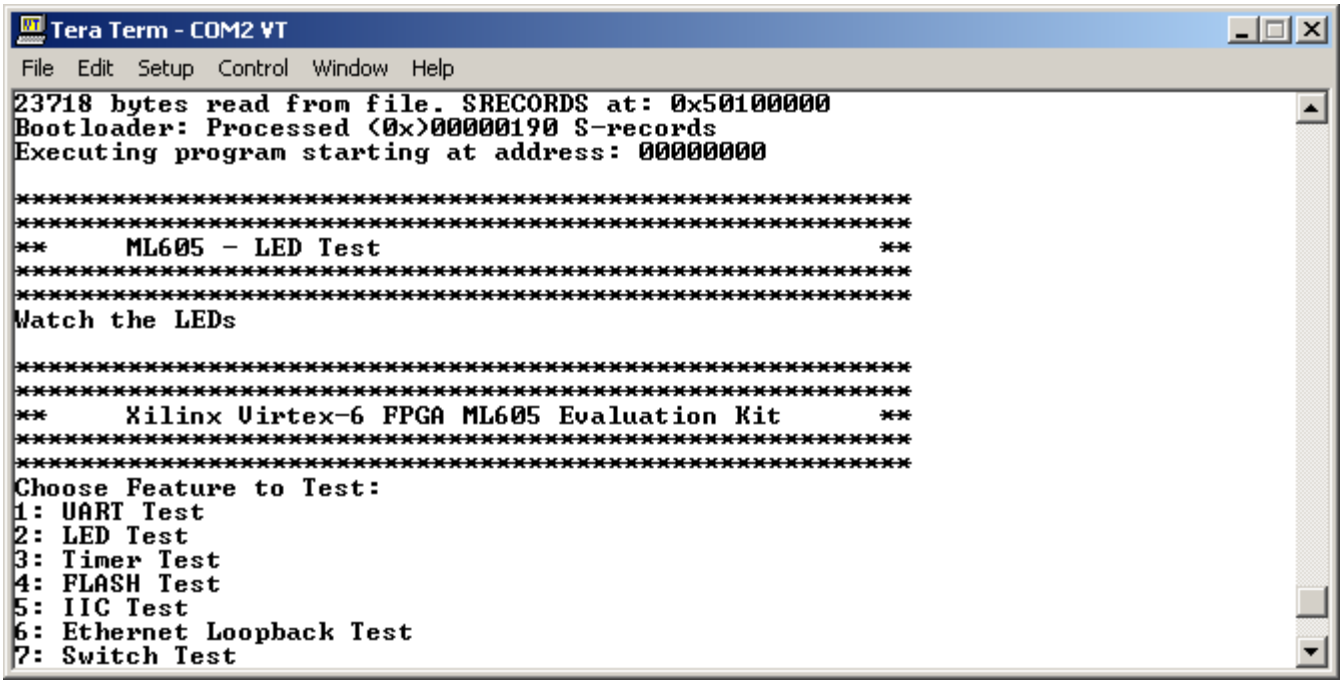


Figure 1-12: **2. LED Test**

12. Type a **3** to start the Timer test.

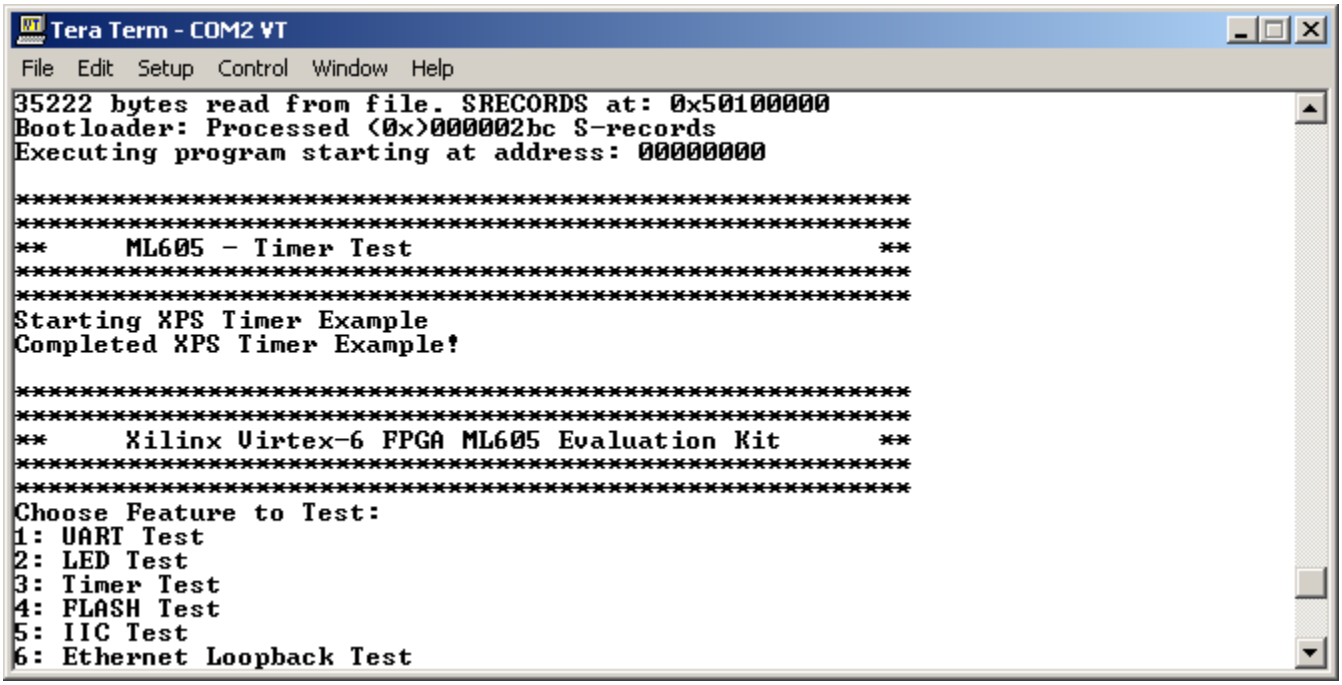


Figure 1-13: **3. Timer Test**

13. Type a **4** to start the flash test.

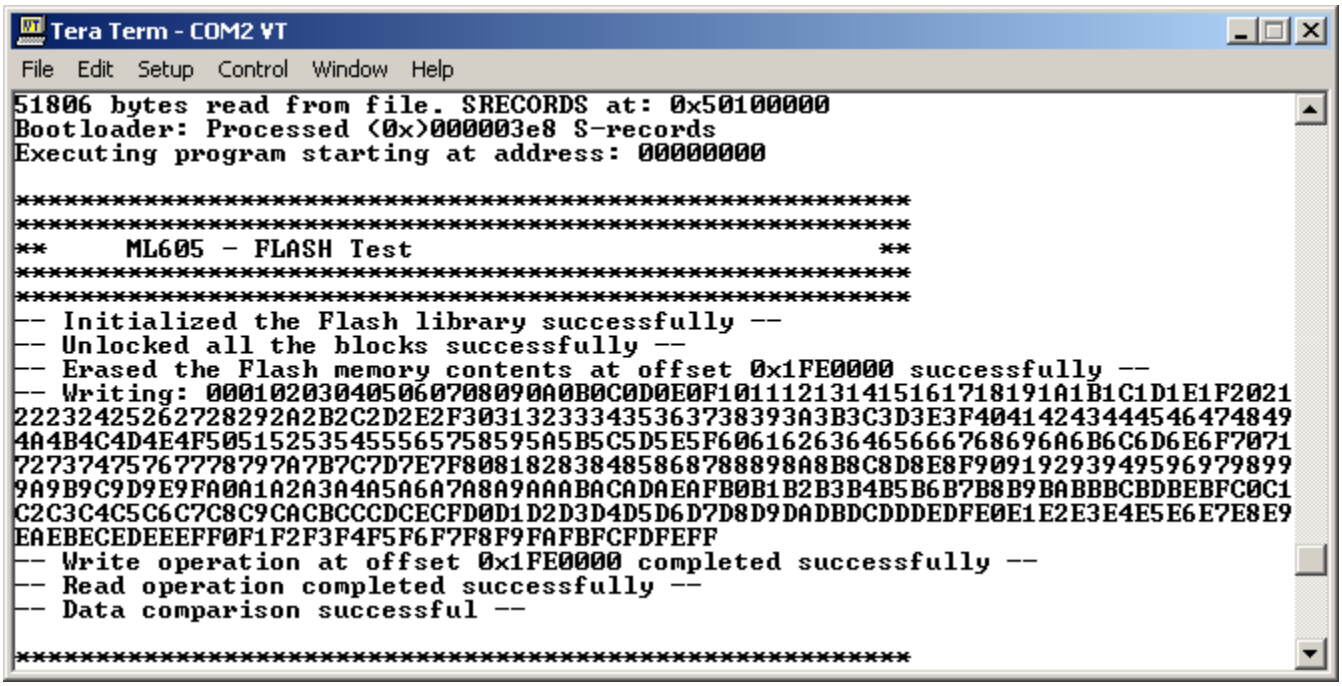


Figure 1-14: **4. Flash Test**

14. Type a **5** to start the IIC EEPROM test.

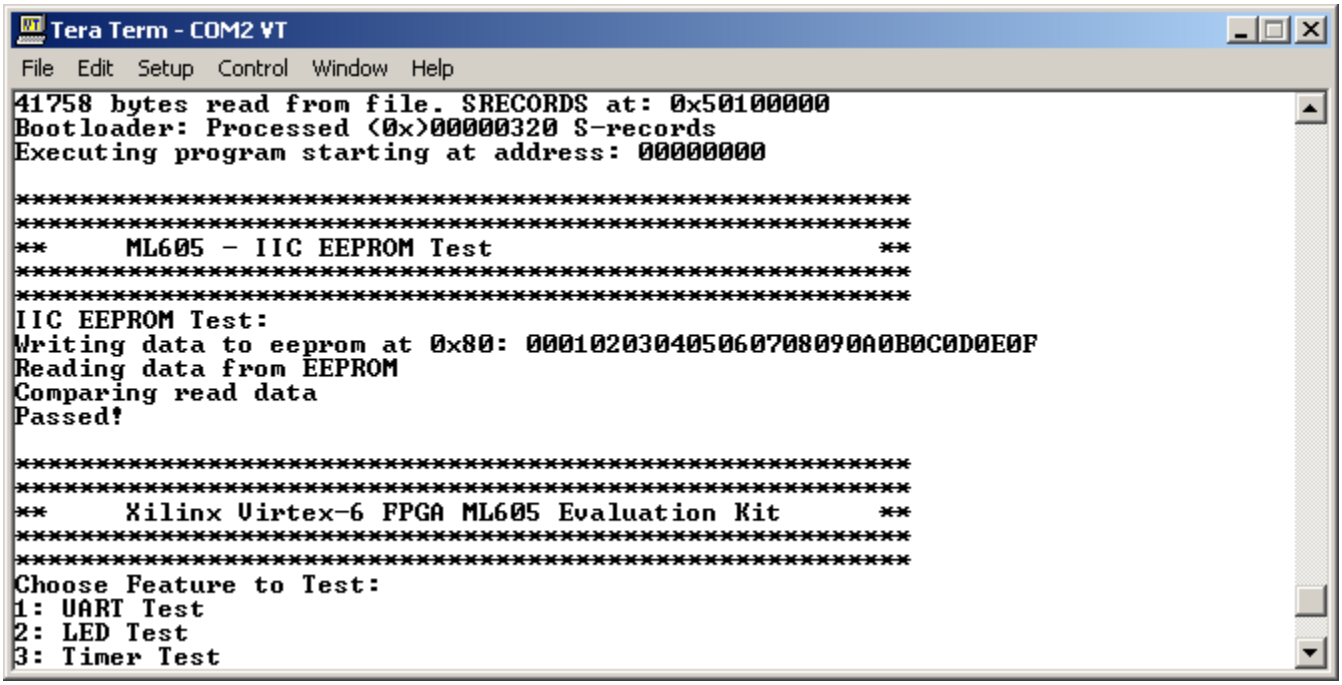


Figure 1-15: **5. IIC EEPROM Test**

15. Type a **6** to start the Ethernet Loopback (Temac) test. This takes approximately 10 seconds to complete.

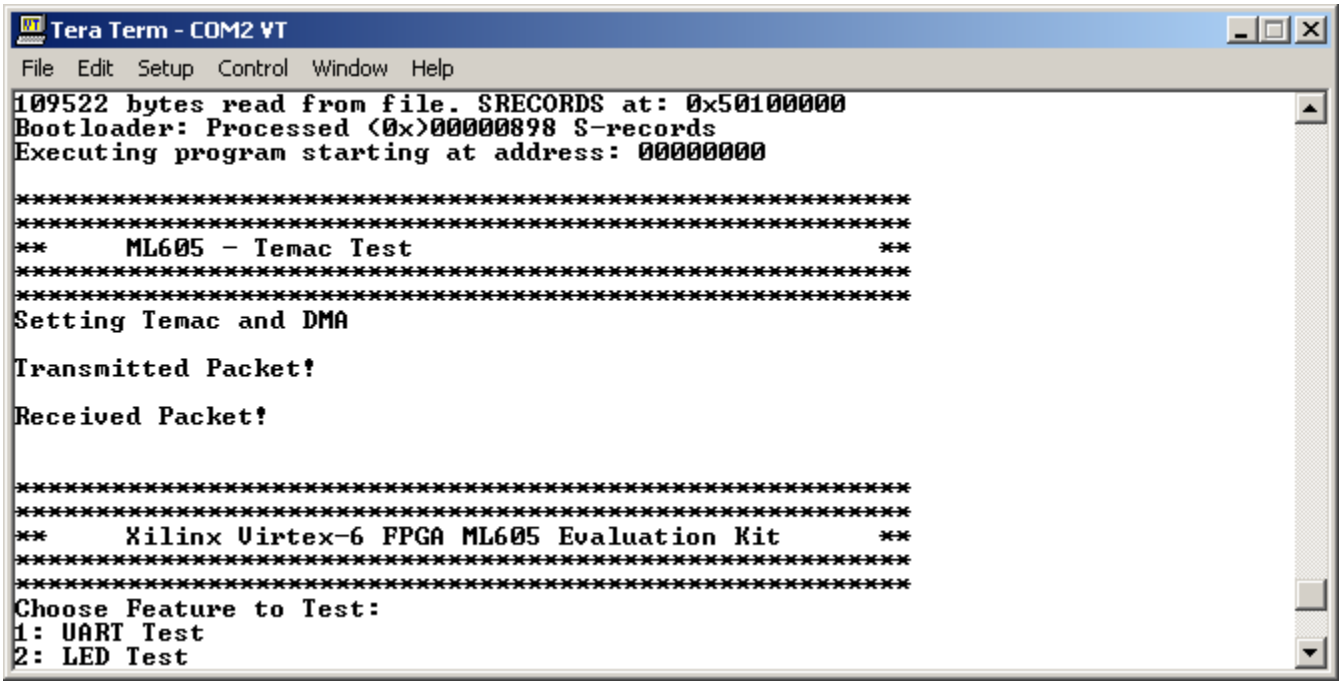


Figure 1-16: **6. Temac Test**

16. Type a **7** to start the GPIO Switch test.

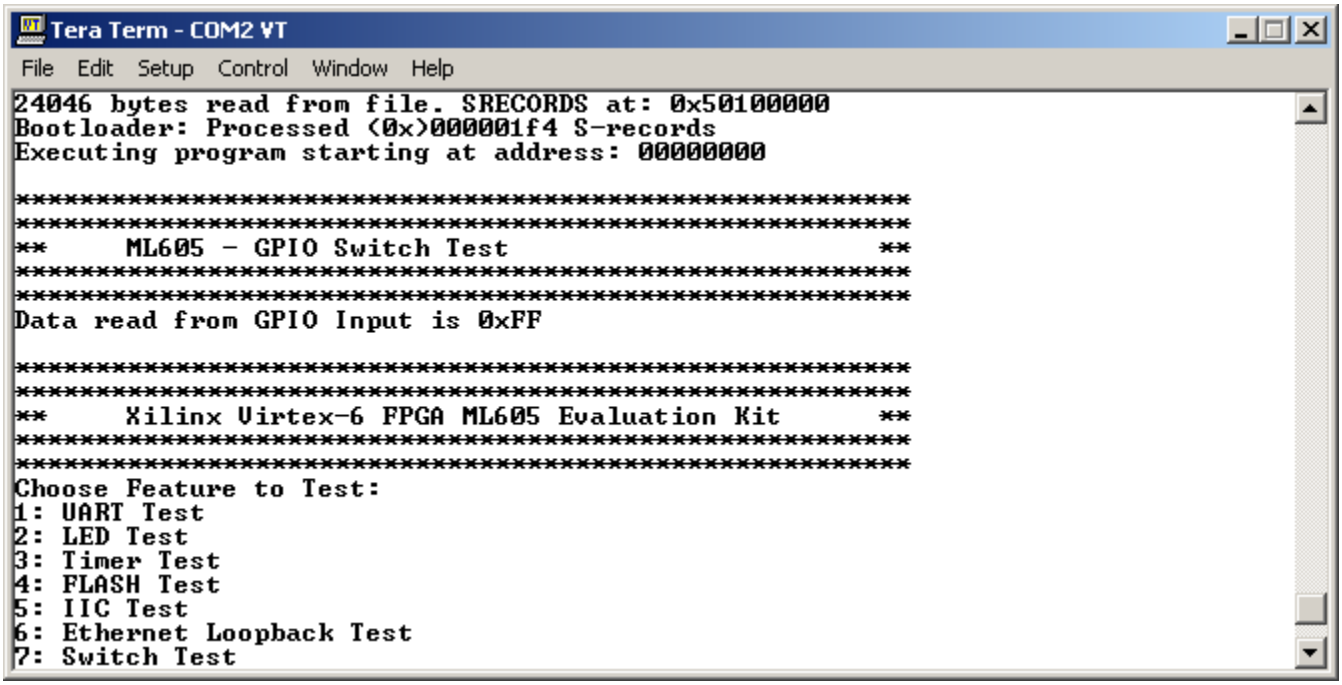


Figure 1-17: **7. GPIO Switch Test**

17. Type an **8** to start the External Memory (Multi-Port Memory Controller, MPMC) test. This takes approximately 20 minutes to complete.

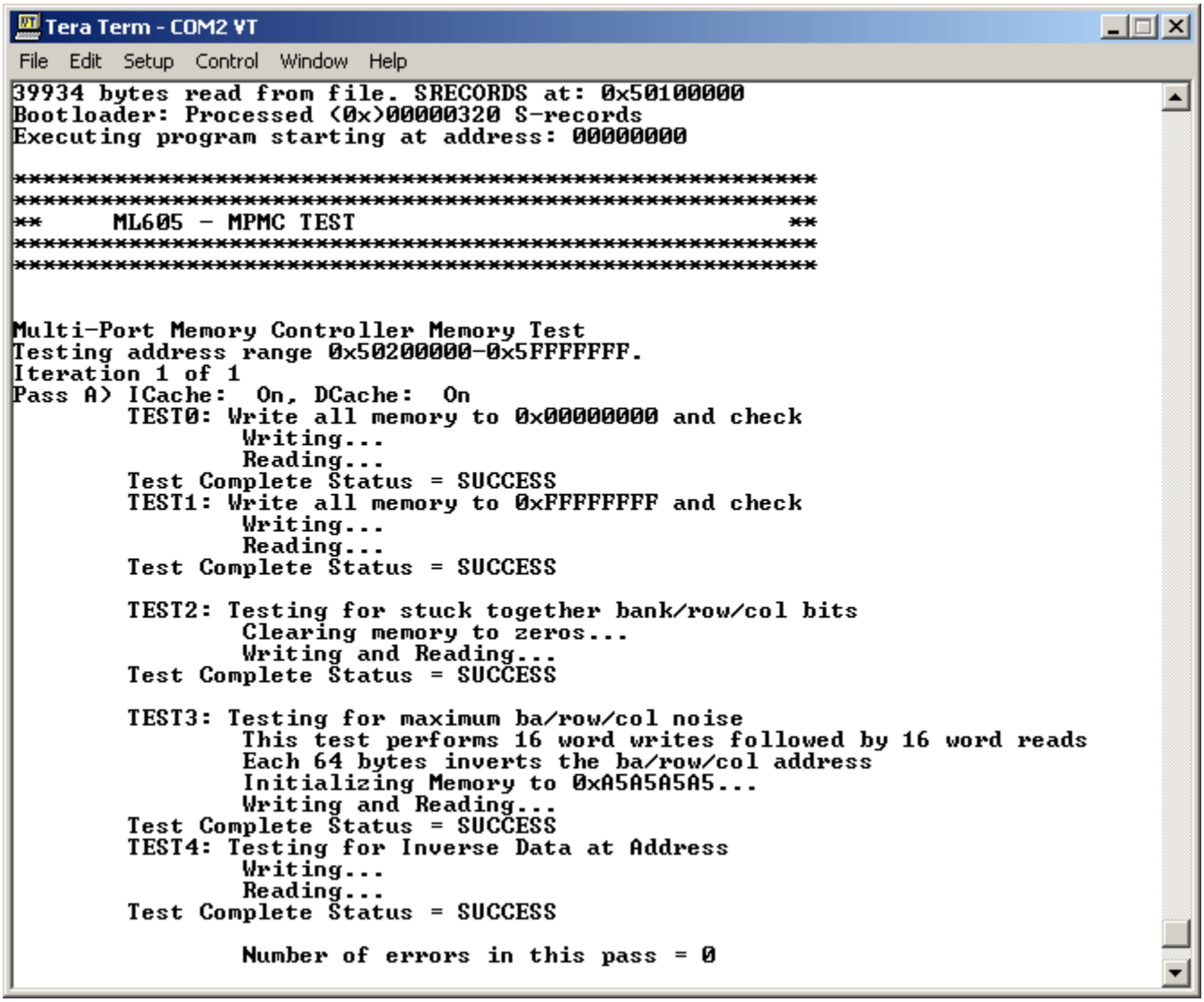


Figure 1-18: **8. MPMC Test**

Figure 1-19 shows the MPMC test status.

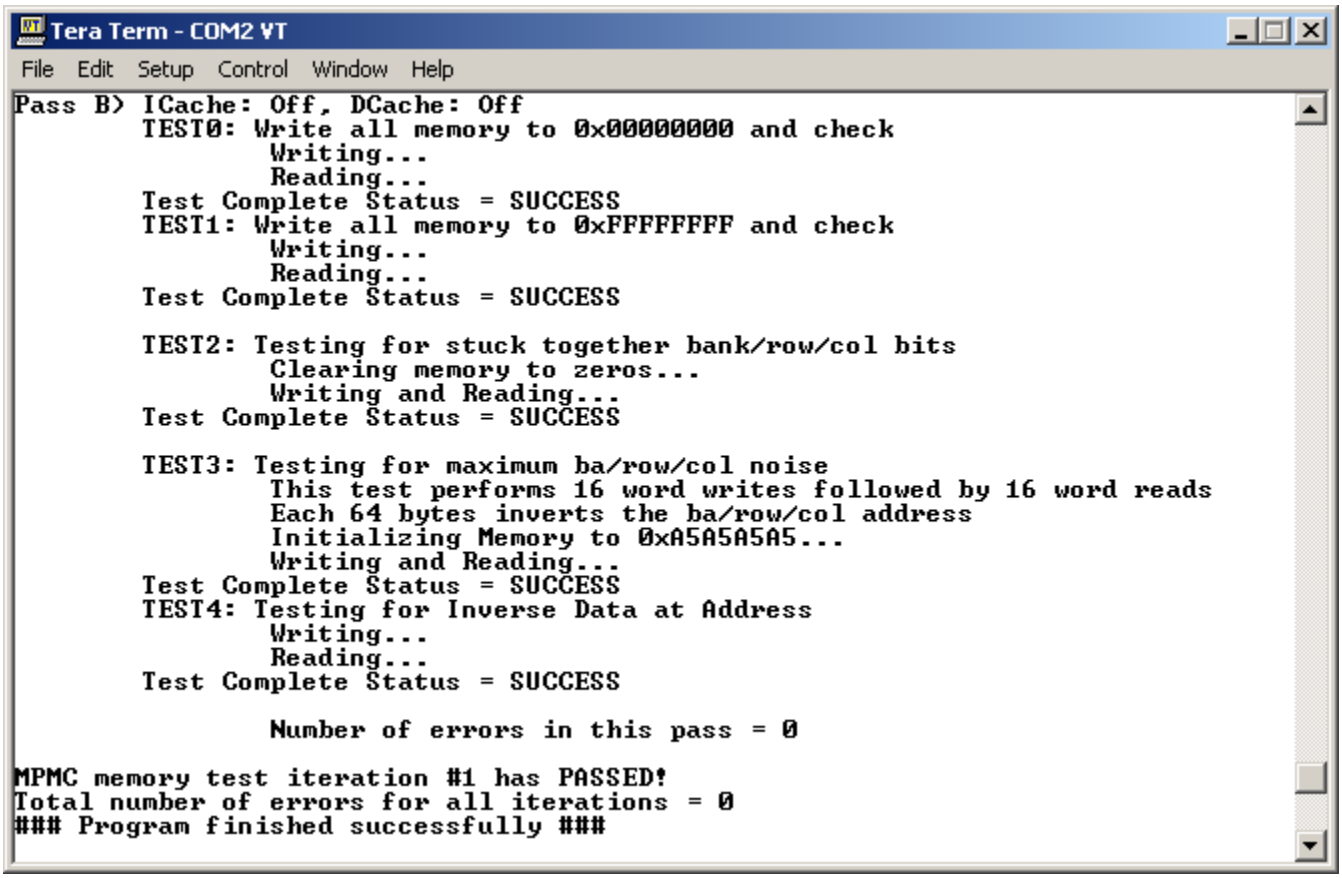


Figure 1-19: **MPMC Test Status**

18. Type a **9** to start the System Monitor test.

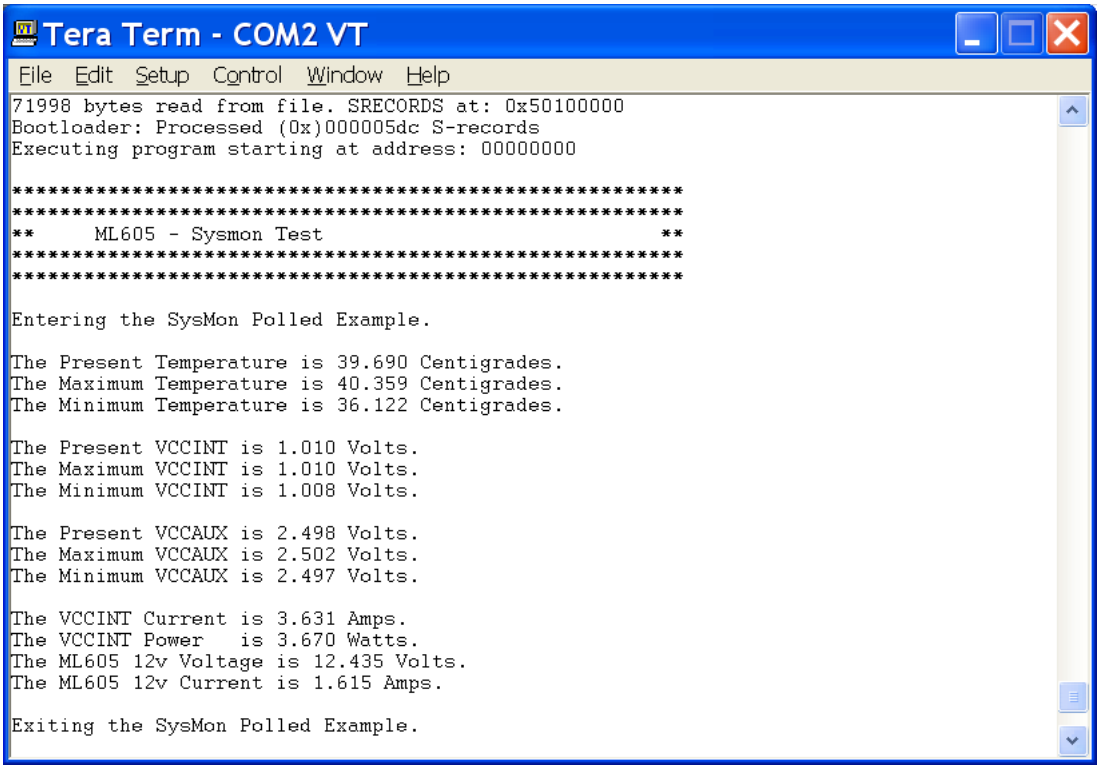


Figure 1-20: **9. System Monitor Test**

19. Type an **A** to test the North, South, East, West, and Center pushbuttons (as shown in Figure 1-21).

Figure 1-21: **ML605 North, South, East, West, and Center Pushbuttons**

Figure 1-22 shows the test menu.

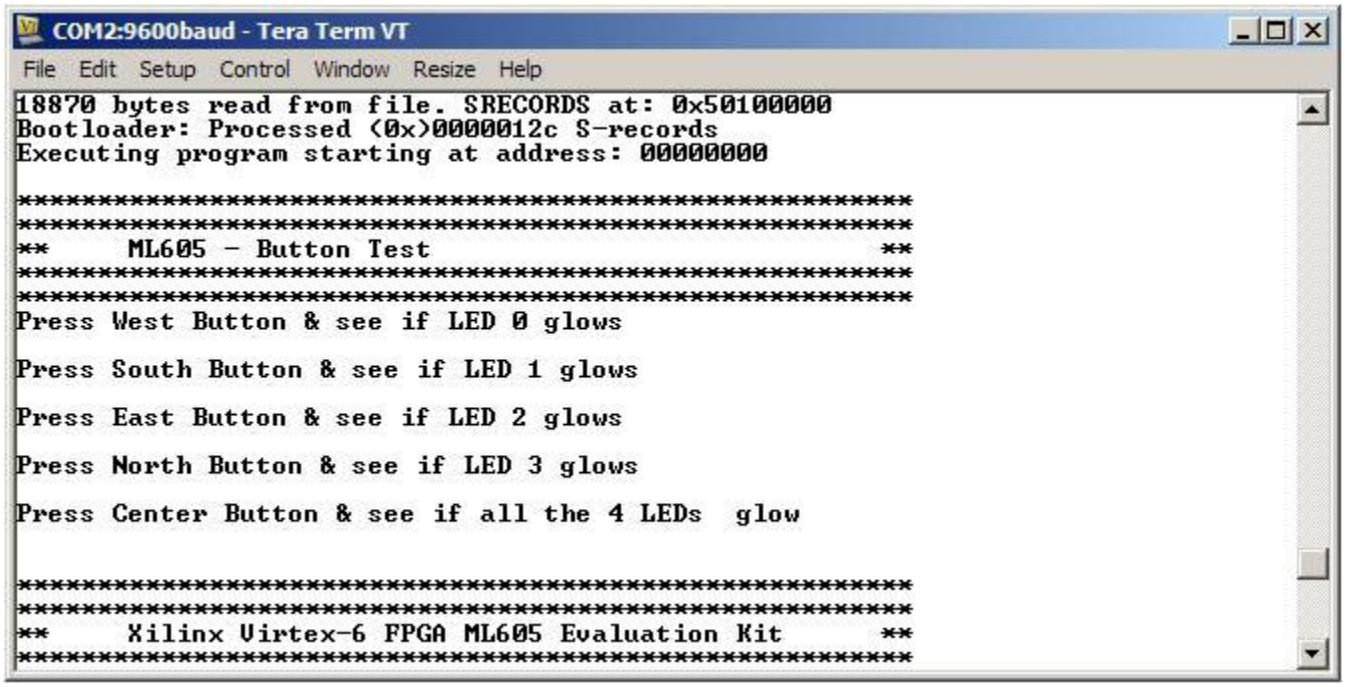


Figure 1-22: **Pushbutton Test**

20. Type a **B** to start the LCD test.

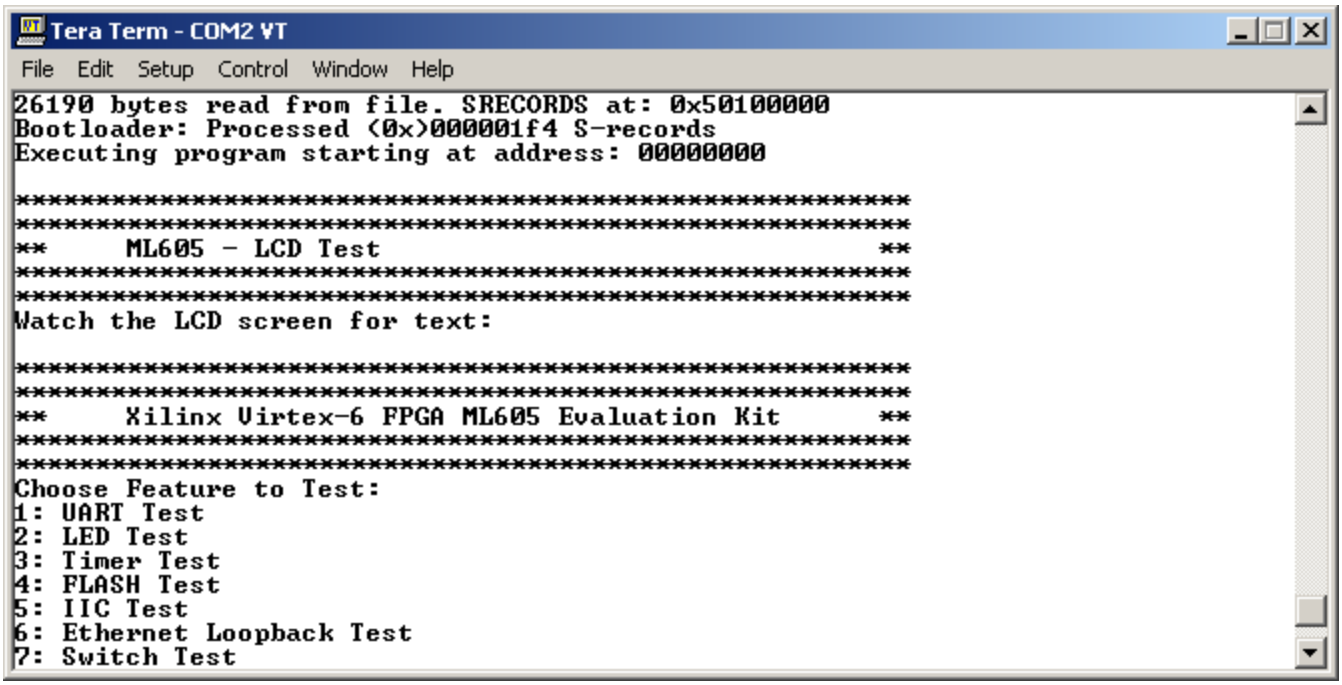


Figure 1-23: **LCD Test**

21. Type a **C** to start the System ACE CF test.

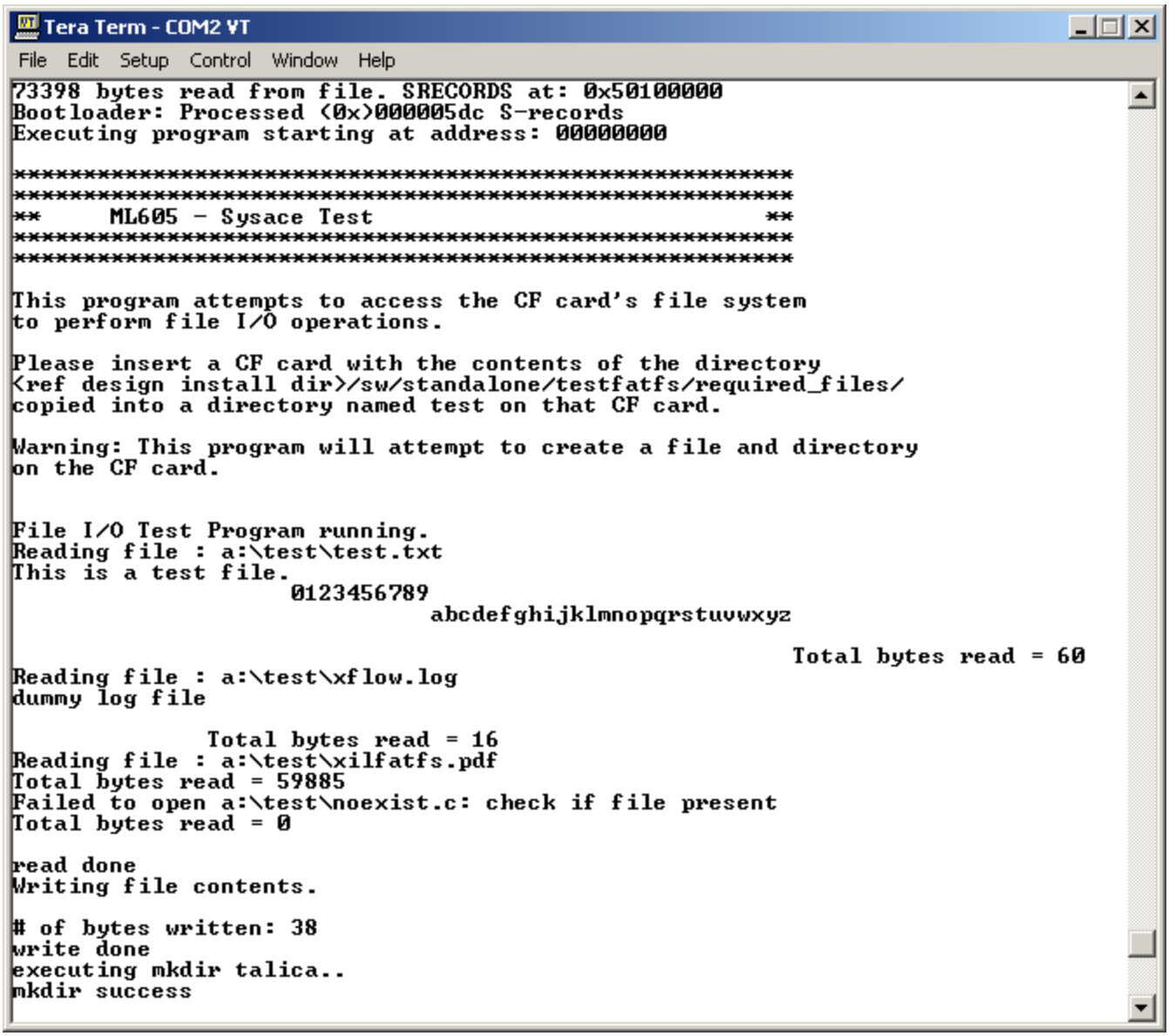


Figure 1-24: **System ACE CF Test**

22. Connect a DVI monitor to the ML605 board using the connector shown in Figure 1-25. The DVI/VGA adapter provided in the ML605 Evaluation Kit can be used to connect a VGA monitor.

Figure 1-25: **ML605 DVI Connector**

23. Type a **D** to start the DVI/VGA (TFT) test. The test patterns indicated in Figure 1-26 appear on the monitor.

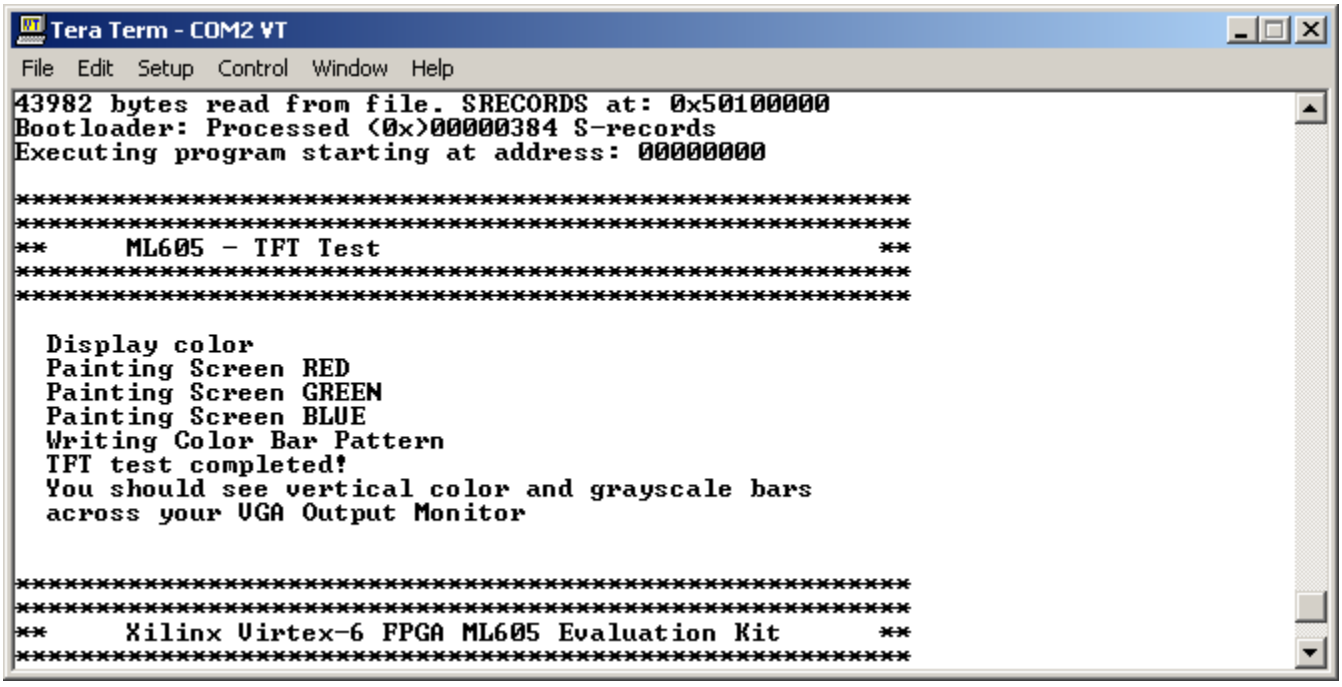


Figure 1-26: **TFT Test**

Getting Started with PCI Express PIO Demonstration

The LogiCORE™ IP Virtex-6 Integrated Block for PCI Express® core is a high-bandwidth, scalable, and reliable serial interconnect building block for use with Virtex-6 FPGA devices. The Integrated Block for PCI Express solution supports 1-lane, 2-lane, 4- lane, and 8-lane Endpoint and Root Port configurations at up to Gen2 speed, all of which are compliant with the *PCI Express Base Specification*, v2.0.

For information about the internal architecture of the Virtex-6 FPGA Integrated Block, see the *LogiCORE™ IP Virtex-6 FPGA Integrated Block User Guide for PCI Express*. [Ref 18]

Figure 1-27 illustrates the interfaces to the core.

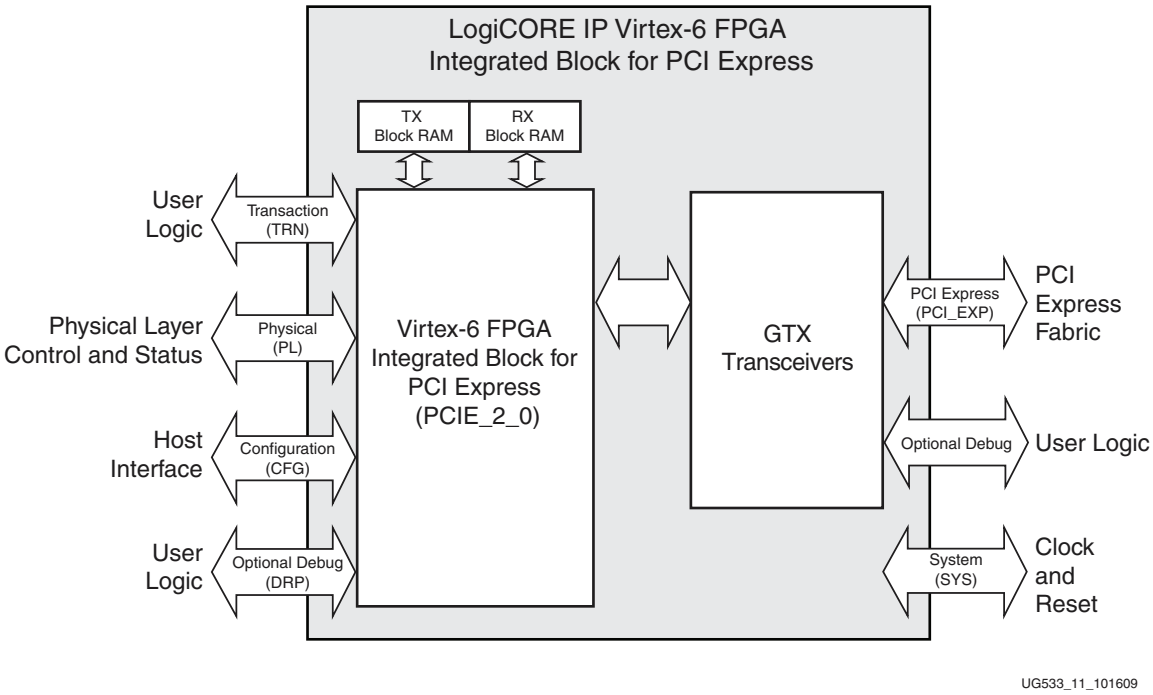


Figure 1-27: **Interfaces to the Core**

The ML605 x8 PCI Express Gen 1 Programmed Input Output (PIO) design consists of a simple example that can accept read and write transactions and respond to requests. PIO transactions are generally used by a PCI Express system host CPU to access Memory Mapped Input Output (MMIO) and Configuration Mapped Input Output (CMIO) locations in the PCI Express fabric. Endpoints for PCI Express accept Memory and IO Write transactions and respond to Memory and IO Read transactions with Completion with Data transactions.

The ML605 PIO example design is included with the Endpoint for PCIe generated by the CORE Generator, which allows users to easily bring up their system board with a known established working design to verify the link and functionality of the board.

The step-by-step procedure for creating the PIO design by Xilinx CORE Generator™ software is illustrated by the *ML605 PCIe x8 Gen1 Design Creation* tutorial [Ref 23]. See http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm.

System Requirements, Installation, and Setup

Software Requirement

PciTree is a graphical Windows tool that can be used for checking the presence of PCI devices in PCIbus.

Software Installation and Setup

1. Download the free PciTree tool (Figure 1-28) from http://www.pcitree.de/download.html
2. Unzip `PCItree.zip` to your folder of choice
3. Click on `PCITree.exe` and proceed with the installation
4. Copy `HLP.SYS` to C:\WINDOWS\system32\drivers directory
5. Verify the installation

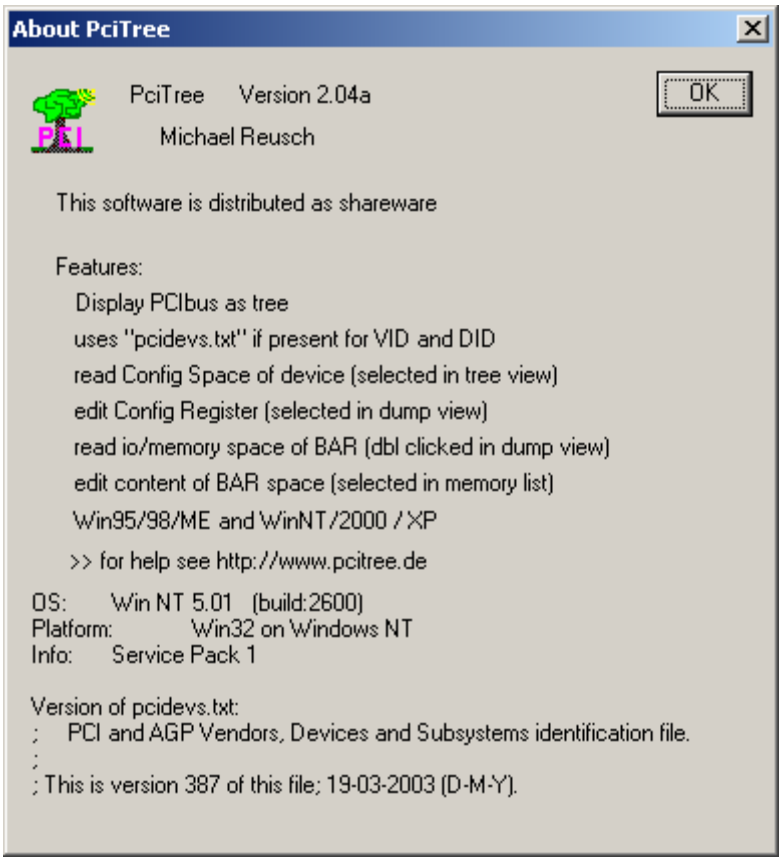


Figure 1-28: **About the PciTree Tool**

Hardware Requirement

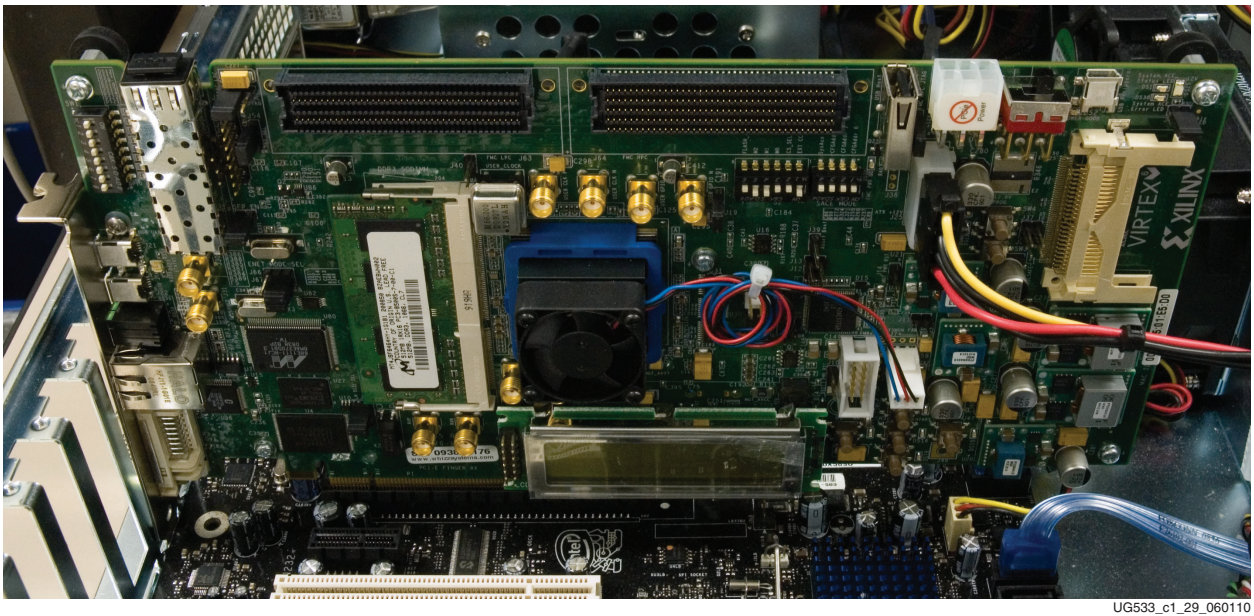
- PC with Gen 1 x8 or x16 PCI Express slot fully dedicated for add-on end-point PCIe card (the slot should not be dedicated to graphic cards only)
- ML605 board

Hardware Installation and Setup

All jumpers on the ML605 should remain set to the factory default. As viewed from left-to-right in Figure 1-29, S2 is set to 011001. This will configure the FPGA from the Platform Flash XL device using Slave SelectMAP and the onboard external oscillator for CCLK. J42 should also have a shunt on pins 5 and 6 for x8 PCI Express configuration.

6. Ensure Configuration Mode Switch S2 is set to 011001 (position 6 to position 1)
7. Insert your ML605 board into a PCIe x8 slot (x16 as shown in Figure 1-29).
8. Connect your PC power to J25 and turn on the power switch.

   Caution! Do not use the PCIe power connector from the PC power supply. Use only the 4-pin ATX connector.



UG533_c1_29_060110

Figure 1-29: **Board Insertion Location**

Running the PCI Express PIO Demonstration

9. Power on your PC and wait for your ML605 board to power up consequently.
10. The x8 PCI Express PIO design is pre-loaded on the ML605 board's Platform Flash XL. Upon the board's power up and successful configuration of the onboard LX240T FPGA, the DONE LED (DS13) should illuminate.
11. Launch the PciTree tool and verify the menu shown in Figure 1-30.

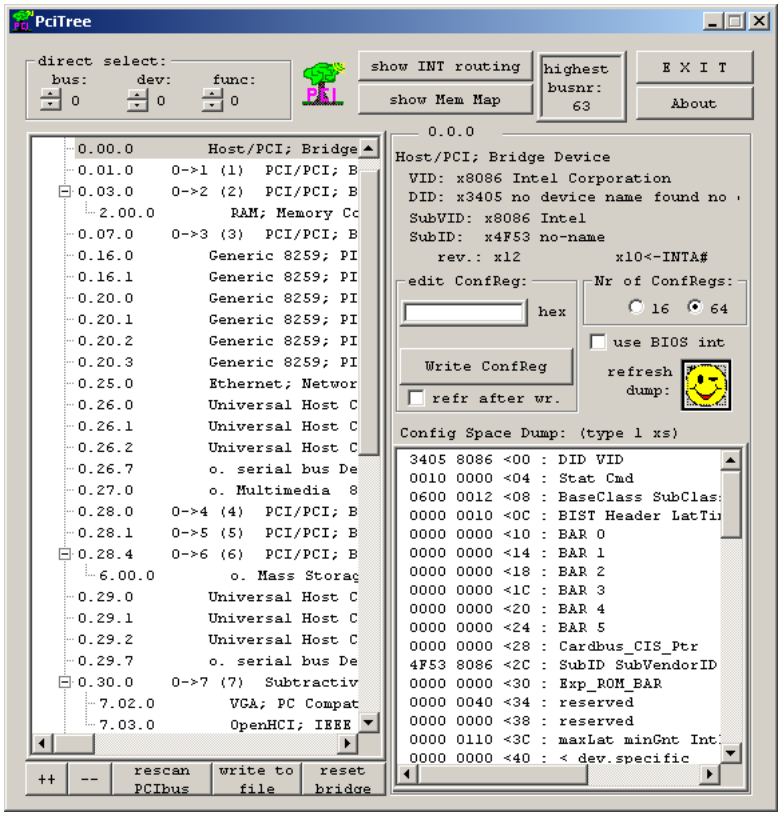


Figure 1-30: **Launch the PciTree Tool**

Configuration Registers Test

12. Set the number of configuration registers to 64 (as shown in Figure 1-31) and click on the **refresh dump:** button.

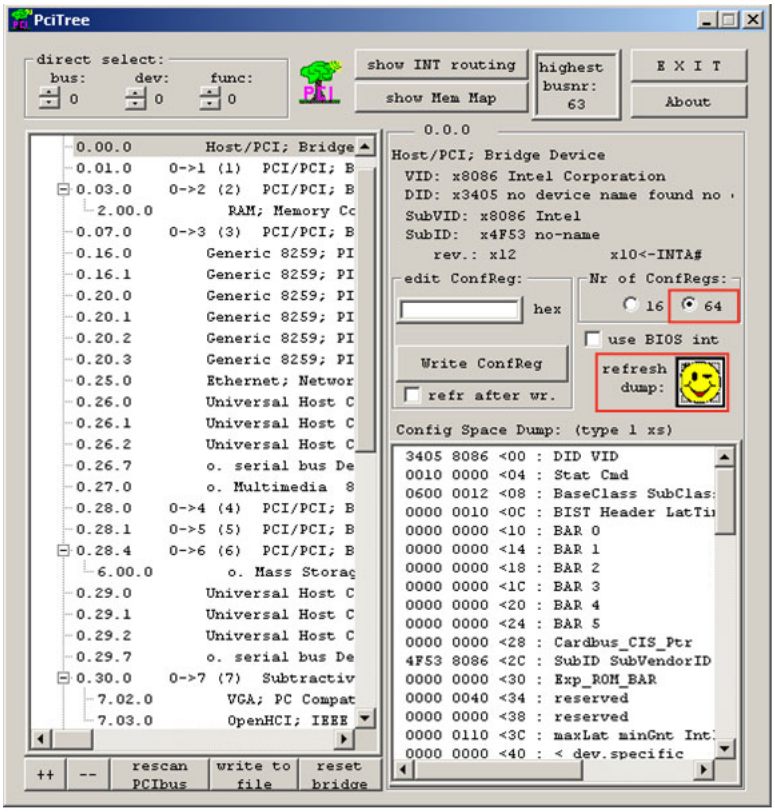


Figure 1-31: **Set Configuration Registers**

13. Locate the Xilinx device as shown in figure Figure 1-32.
    - Xilinx PCI vendor ID is 0x10EE
    - Device ID of the x8 Gen1 configuration is 0x6018

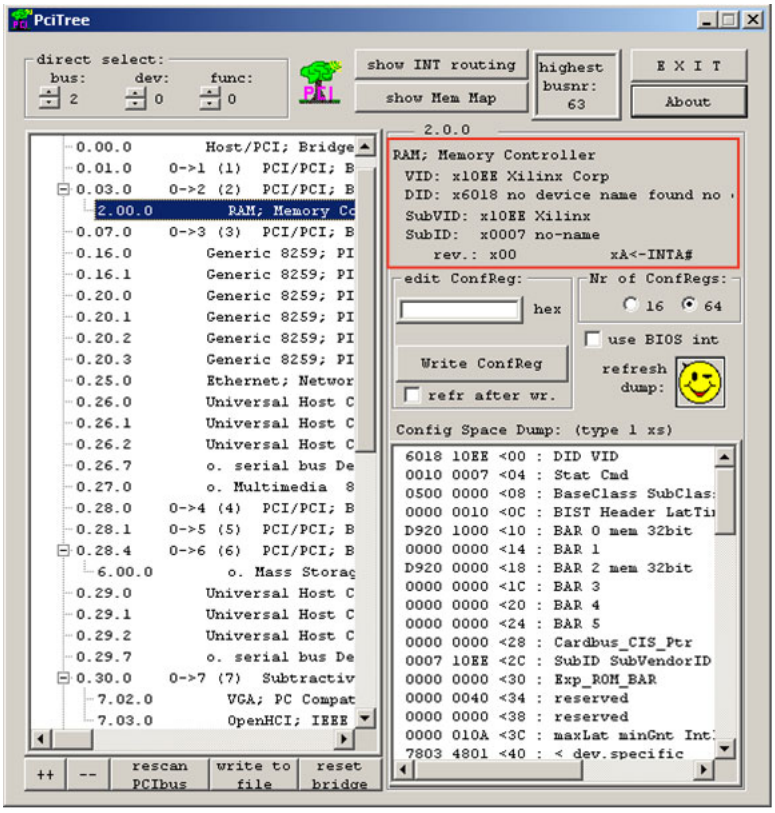


Figure 1-32: **Locate the Xilinx Device**

14. Navigate to the linked list in the configuration space (as shown in Figure 1-33) to locate the PCIe capabilities structure.
15. With the Xilinx device selected, select register 0x40.
    - Register 0x40 points to the next structure
    - 0x48 is the address of the next structure

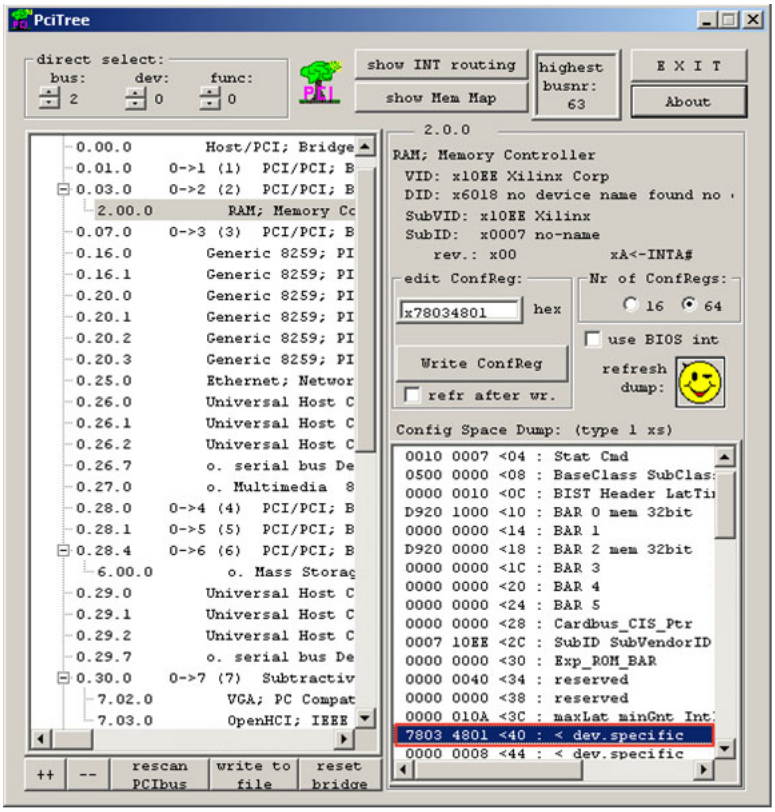


Figure 1-33: **Locate the PCIe Capabilities Structure**

16. Select register 0x48 (as shown in Figure 1-34).
    - Register 0x48 points to the next structure
    - 0x60 is the address of the next structure, indicating the data at this offset is the PCIe Capabilities Structure.

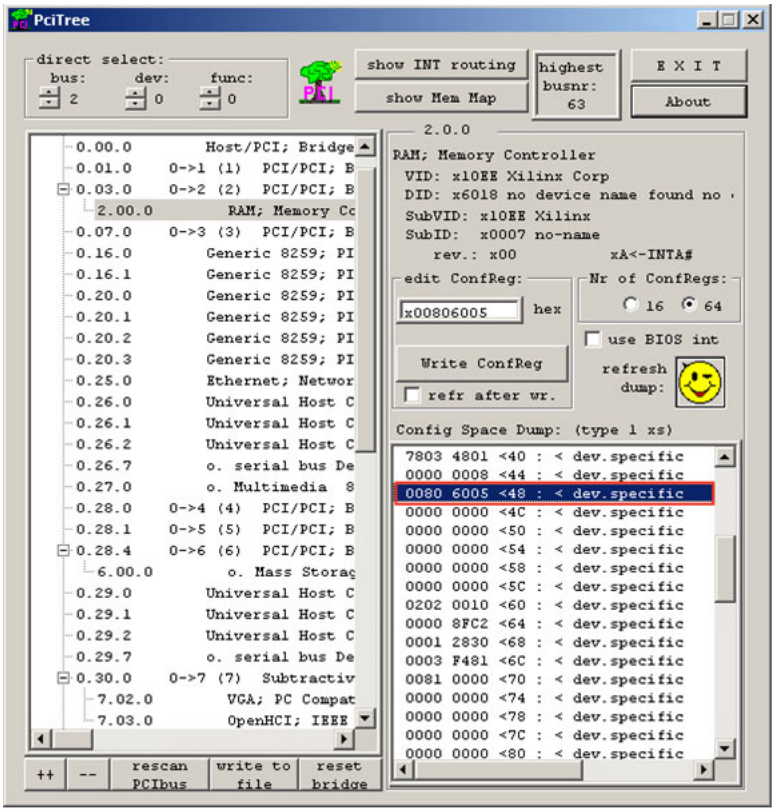


Figure 1-34: **Select Register 0x48**

17. Select register 0x60 (as shown in Figure 1-35).
    - 0x60 is a type 0x10

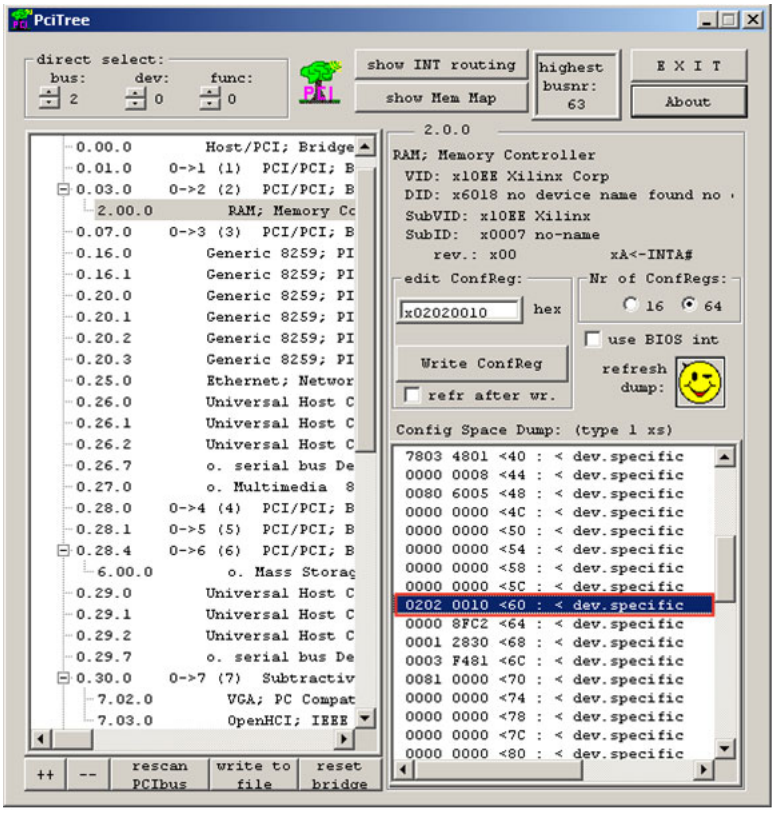


Figure 1-35: **Select Register "0x60"**

18. Select register 0x6C, Link Capabilities Register (Figure 1-36).
    - Indicates the maximum number of lanes and speed supported
    - The value 0x81 shows this is an x8 Gen1 capable device

    The Link Status Register (0x70) shows the current link status
    - This design is trained to Gen1 x8 as indicated by 0x81

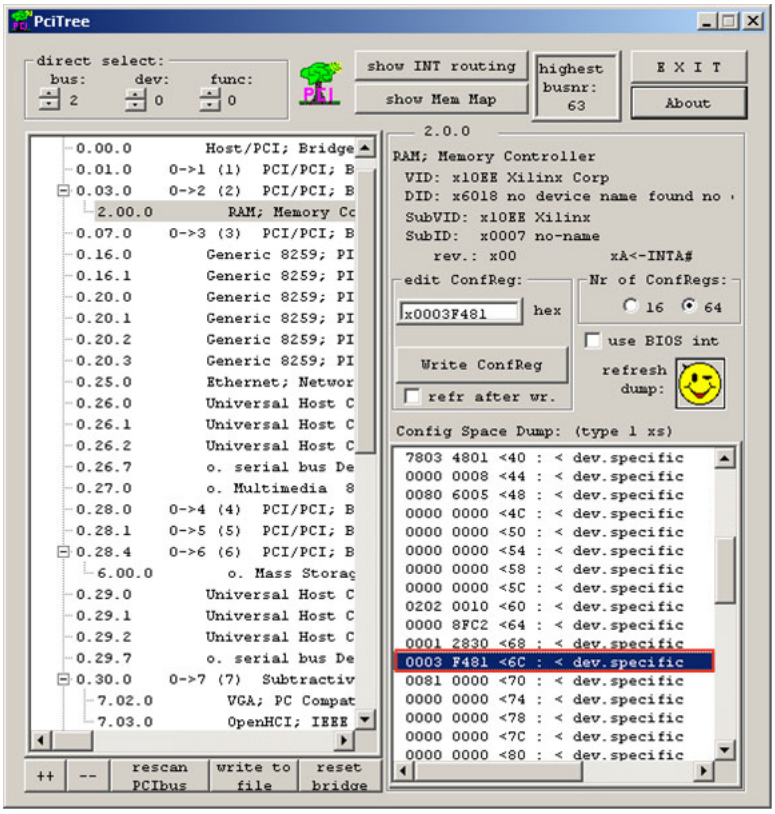


Figure 1-36: **Select Register 0x6C**

Base Address Register (BAR) Test

19. Double-click on BAR 0 (as shown in Figure 1-37).
    - BAR 0 address is machine dependent

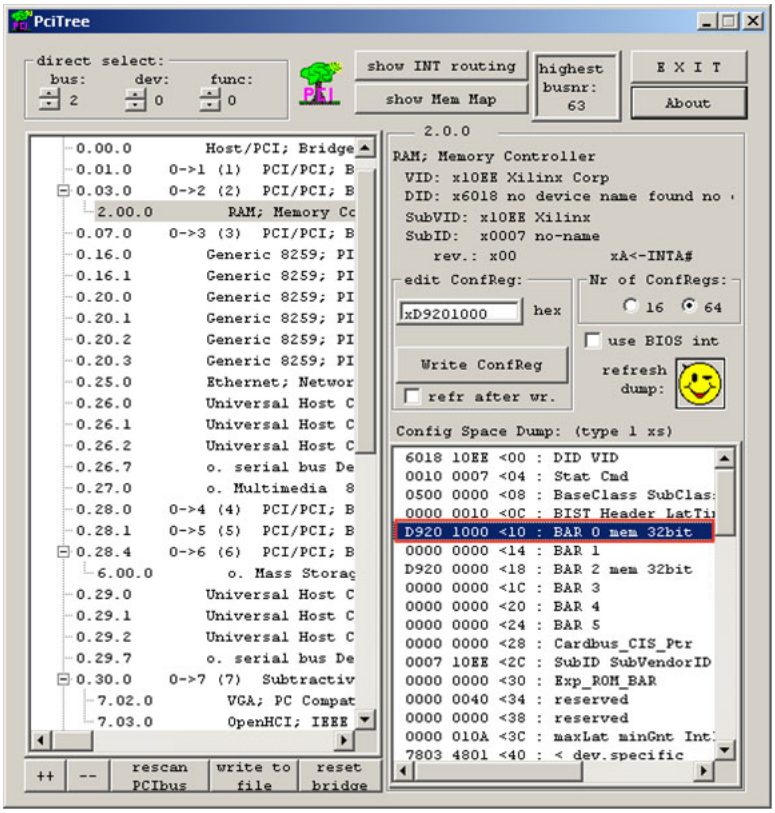


Figure 1-37: **Double-Click on BAR 0**

20. Click Yes on the dialog box (as shown in Figure 1-38).

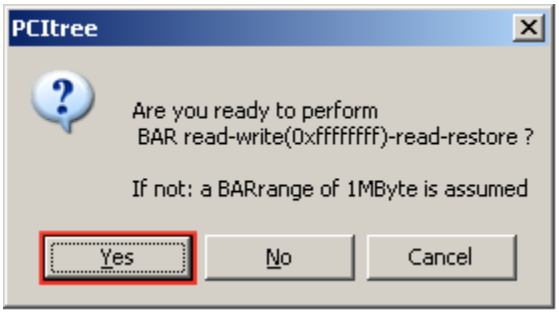


Figure 1-38: **Click Yes**

21. Select auto read memory (as shown in Figure 1-39).

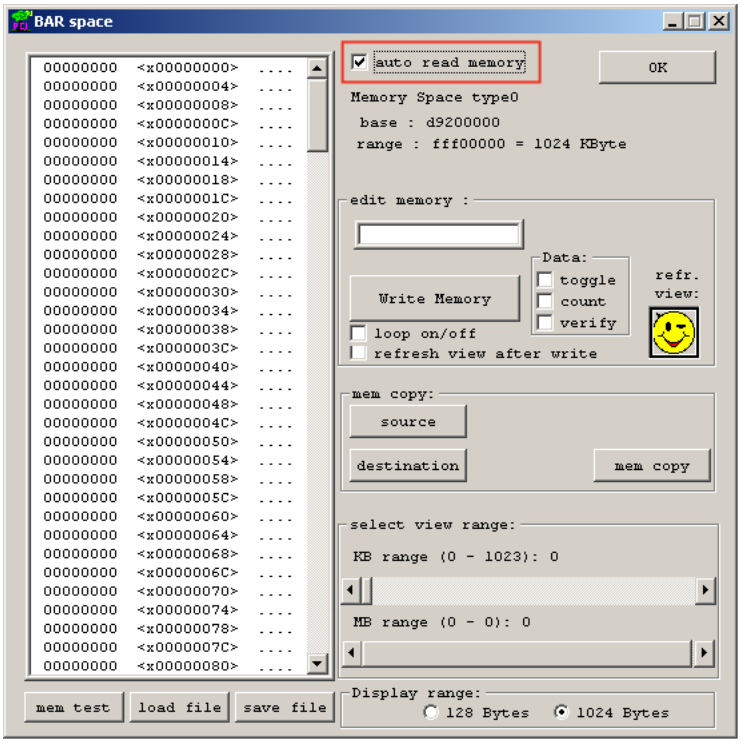


Figure 1-39: **Select Auto Read Memory**

22. Click on the first memory location by holding <Shift-End> keys. This will select 1024 bytes as shown in Figure 1-40.

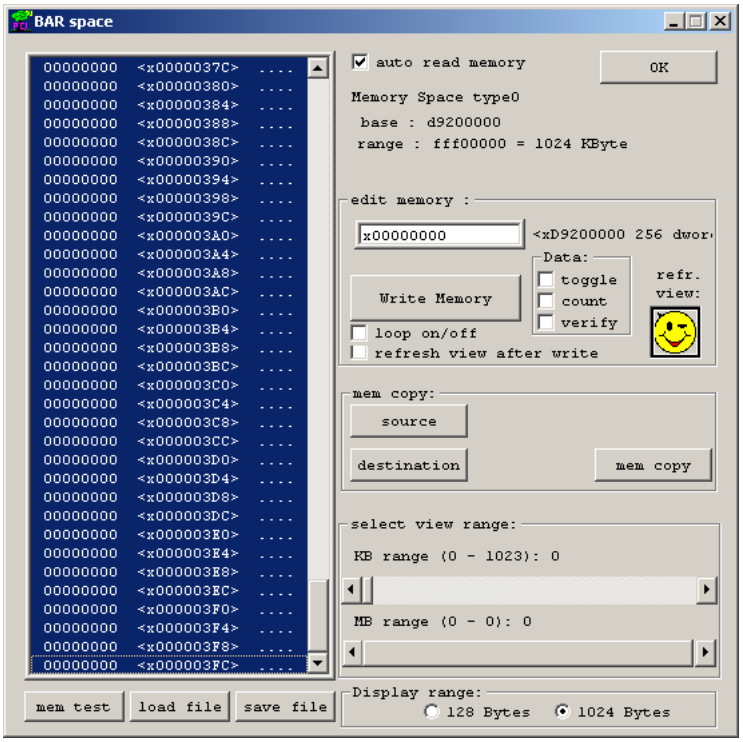


Figure 1-40: **Select 1024 Bytes**

23. Write to memory by selecting the count box and Write Memory button (as shown in Figure 1-41).
24. Verify the result (counting up to FF) by selecting the **refr. view:** button.

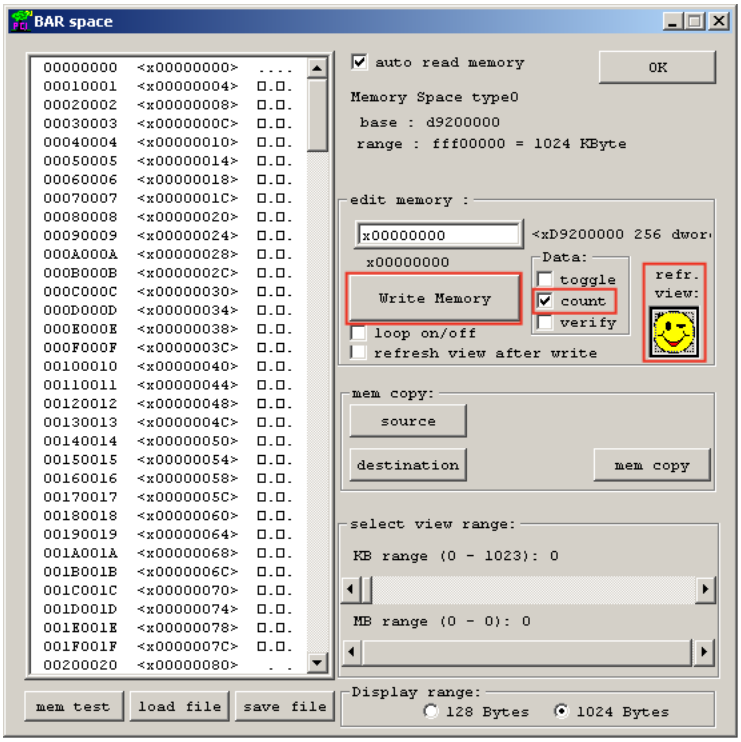


Figure 1-41: **Select to Write Memory**

25. Restore the memory by deselecting the count box and clicking the Write Memory button (as shown in Figure 1-42).
26. Review the result by clicking on the **refr. view:** button.

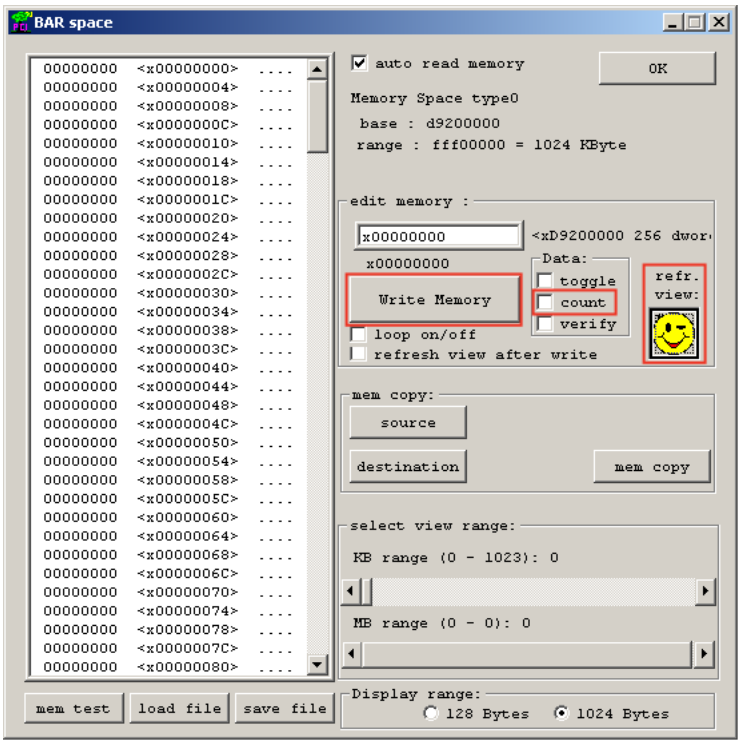


Figure 1-42: **Restore Memory**

Getting Started with the Base Reference Design

The Base Reference Design targeting the ML605 evaluation board, will filter images that are transferred via Ethernet between the evaluation board and a PC. The images are stored in DDR3 SDRAM available on the evaluation board. The stored image is continuously read from SDRAM and filtered by the LX240T FPGA. The resulting image is continuously stored back in the DDR3 SDRAM. This filtered image is then retrieved by the Base Reference Design Interface Software and displayed on a PC.

Figure 1-43 shows a block diagram of the base reference design that has been implemented in the Virtex-6 LX240T FPGA. The reference design includes common functions for Ethernet SGMII communication, external memory interface, UART, and control.

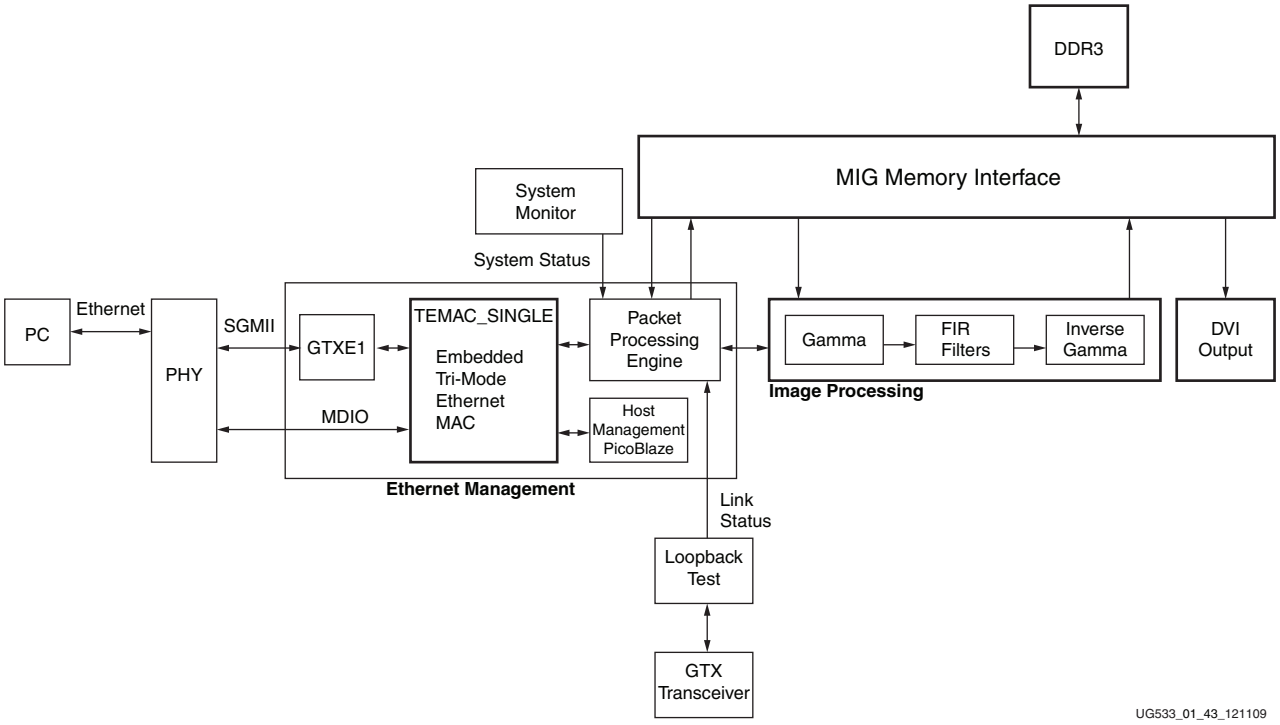


Figure 1-43: **Base Reference Design Block Diagram**

A DDR3 Memory Controller Block is used to store both the unfiltered and filtered images in the DDR3 SDRAM. These images are sent from a PC via a series of Ethernet packets. This memory controller is continuously reading, filtering, and storing images back into this memory. The PC also periodically retrieves the filtered images via Ethernet for display. The Ethernet Management section includes an on-chip hard coded MAC and a Packet Processing Engine. This section provides a way to control various aspects of the demo, transfer images between the demo board and a PC, and receive status from the demo. A simple MDIO controller is implemented using a Xilinx PicoBlaze™ processor. The purpose of this controller is to determine presence of an Ethernet link as well as its operating speed.

The Image Processing structure consists of a 5x5 pixel 2D FIR filter.

Setting up the Hardware for the Base Reference Design

1. Power-off the ML605
2. Connect one end of the provided Ethernet cable to the RJ45 connector P2 on the ML605 and the other end to the Ethernet port on your PC. This connection will be used for communication between the ML605 board and your PC.
3. Set the Ethernet Jumpers for SGMII mode
   - J66: Shunt over pins 2 and 3
   - J67: Shunt over pins 2 and 3
   - J68: No shunt
4. Insert the provided CompactFlash (CF) card into the ML605 CF reader (U73)
5. Set the SACE MODE switch S1 to 1011 (Position 4 to Position 1). This will configure the FPGA from the ACE file stored at configuration address 3 on the CF card
6. Do not change any other factory default settings
7. Power-on the ML605

Installing Base Reference Design Application GUI

The Base Reference Design includes an application GUI that must be installed before you will be able to run the demo. Locate the USB flash drive shipped with your ML605 evaluation kit. Insert the USB drive into your PC and using Windows Explorer, navigate to the USB drive. You should see the following directory structure:

```
ML605_BRD_Application
ML605_BRD_Images
ML605_BRD_Src
Ready_For_Download
```

Note: As an option, you can copy all the necessary files, directories, and images to a local directory on a PC.

Navigate into the ML605_BRD_Application directory. In there you will find an install image, BaseRefDISetup2_0_6.msi. This is an application GUI that is used to display the graphical information for the Base Reference Design. Please double click on this application to install the software.

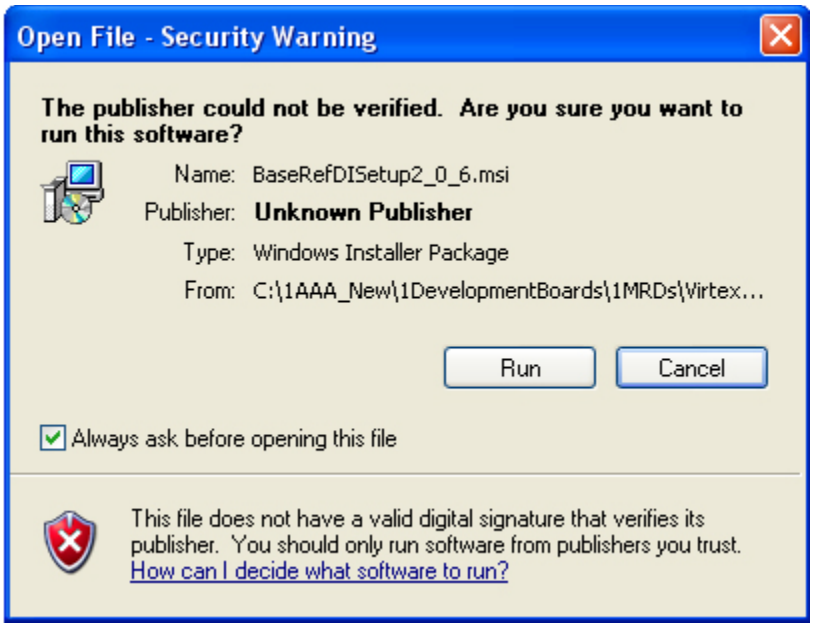


Figure 1-44: **Run BRD GUI Installer**

Click **Run**.

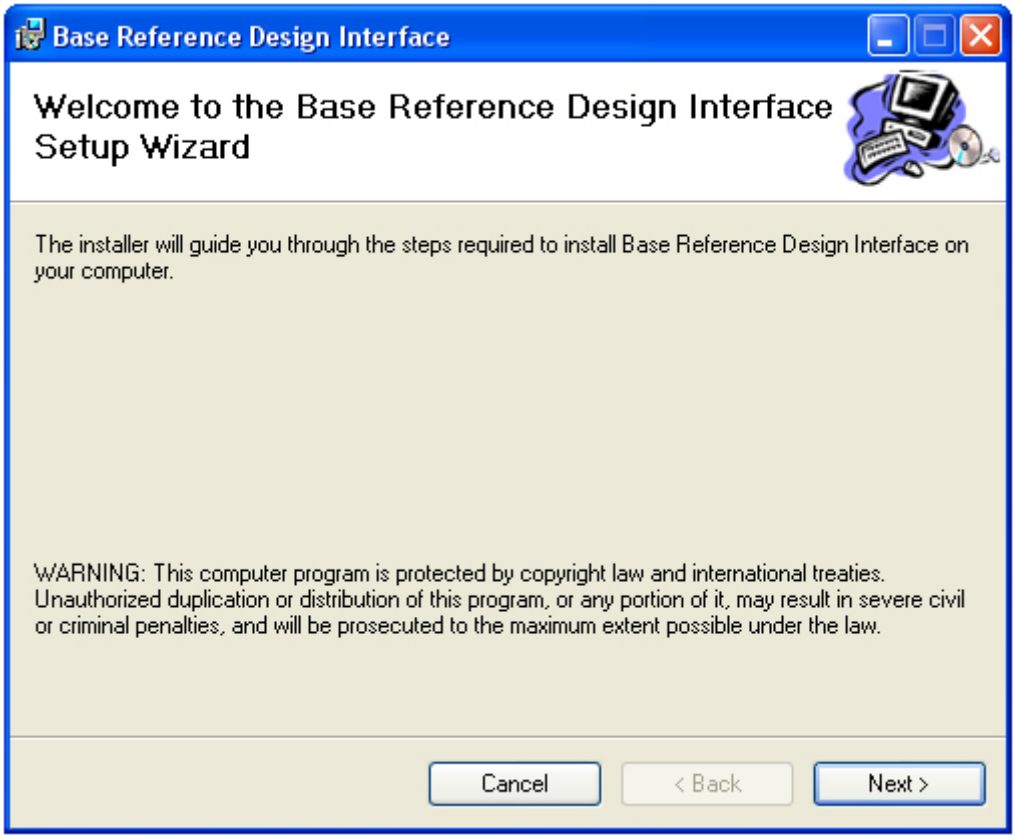


Figure 1-45: **BRD Interface Setup**

Click **Next** to run the BRD Setup Wizard.

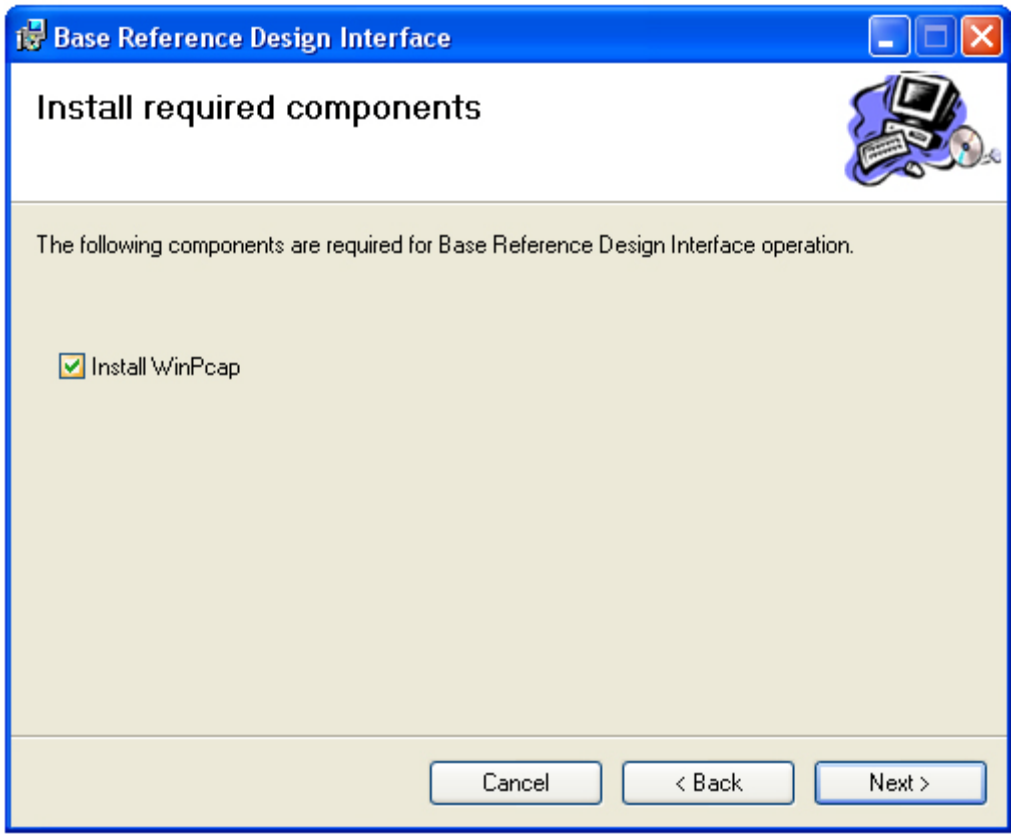


Figure 1-46: **Install Required WinPcap Component**

Click **Next**.

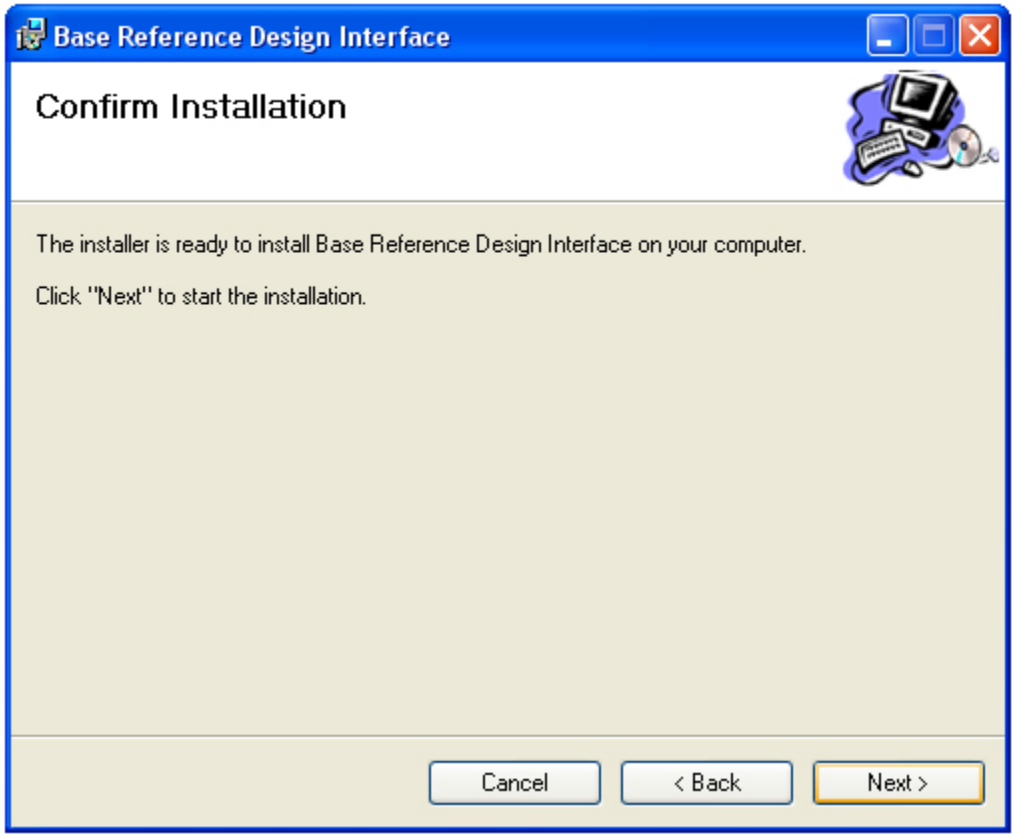


Figure 1-47: **Confirm BRD Installation**

Confirm the Installation by clicking **Next**.

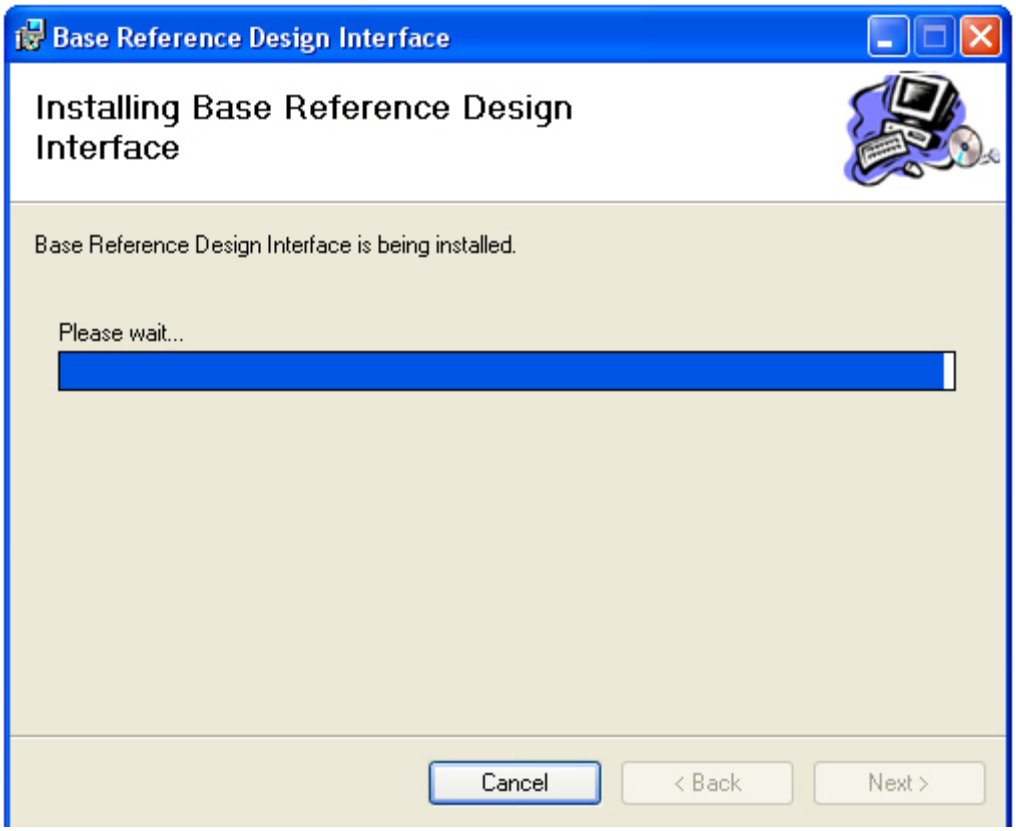


Figure 1-48: **BRD Installation in Progress**

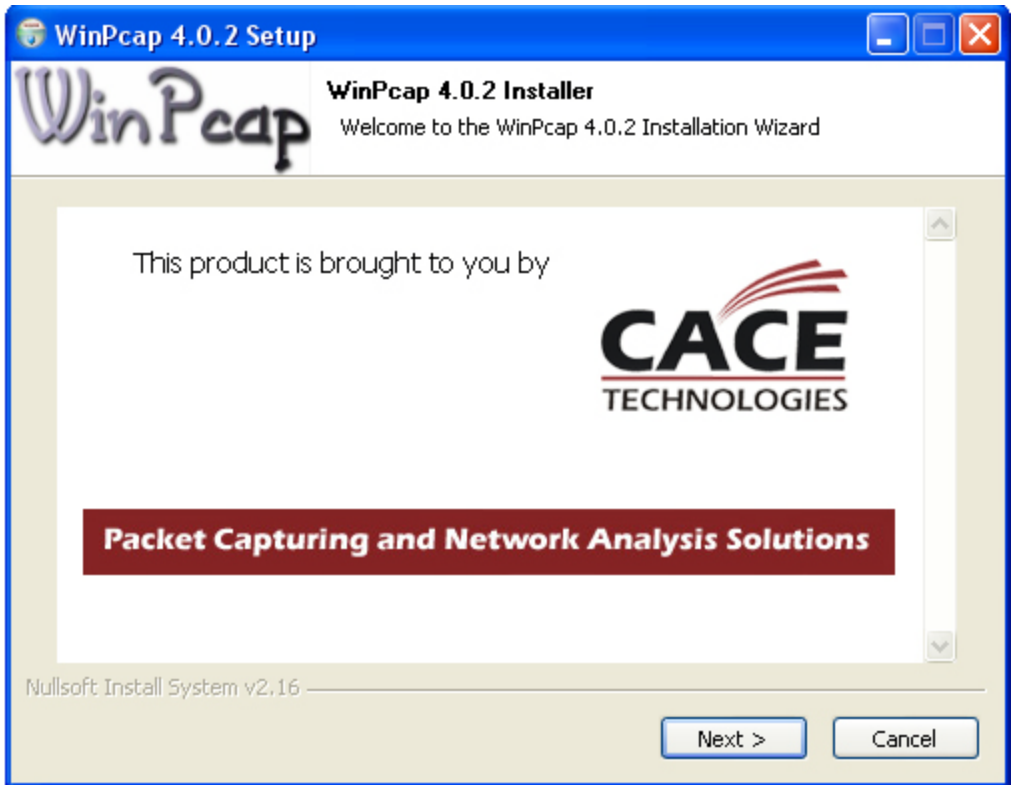


Figure 1-49: **Launch WinPcap Installer**

Click **Next**.

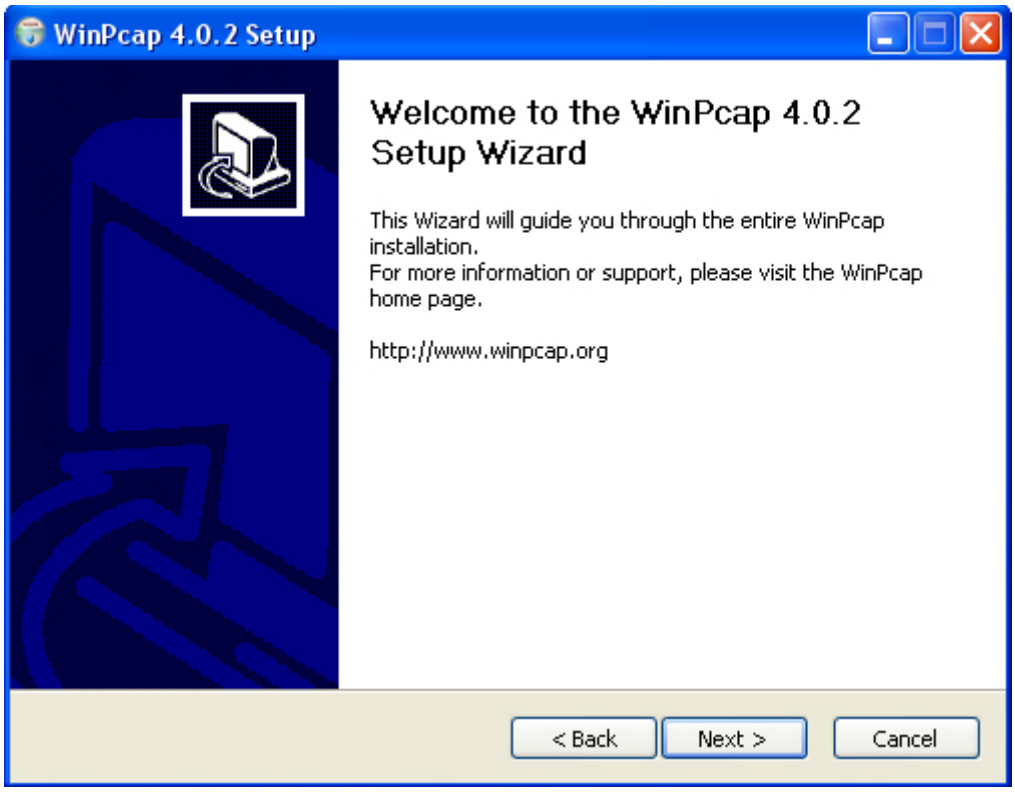


Figure 1-50: **WinPcap Installation Wizard**

Click **Next**.

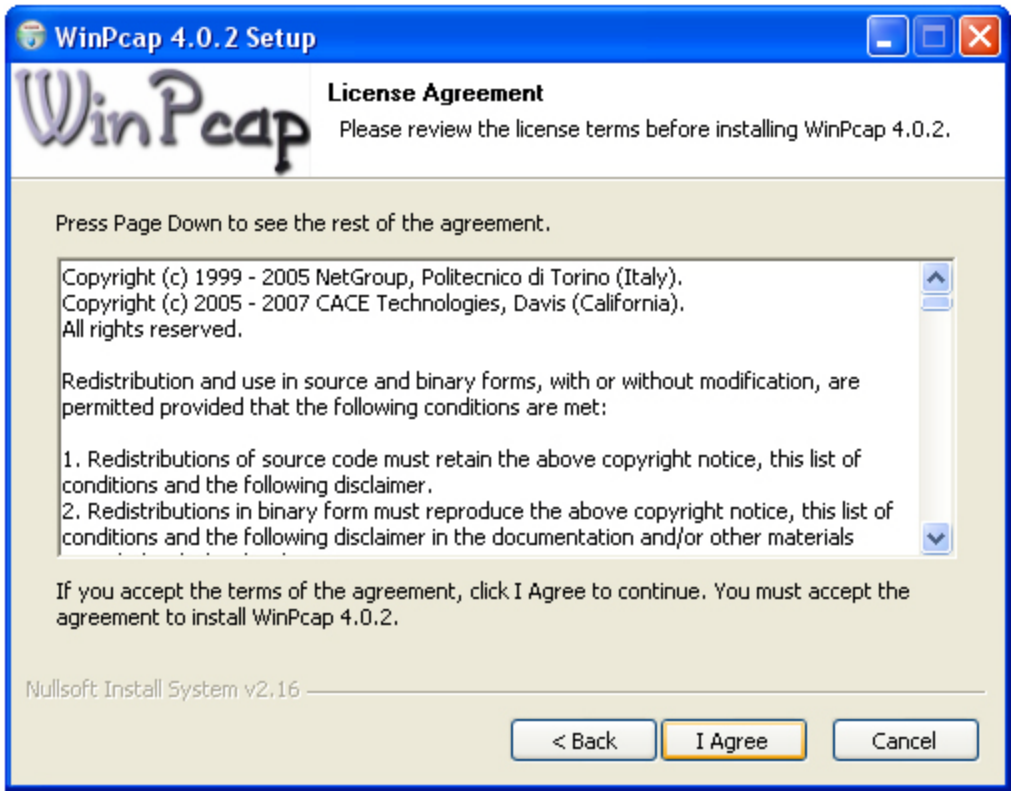


Figure 1-51: **WinPcap License Agreement**

Click **I Agree** if you agree with the WinPCAP license terms and conditions.

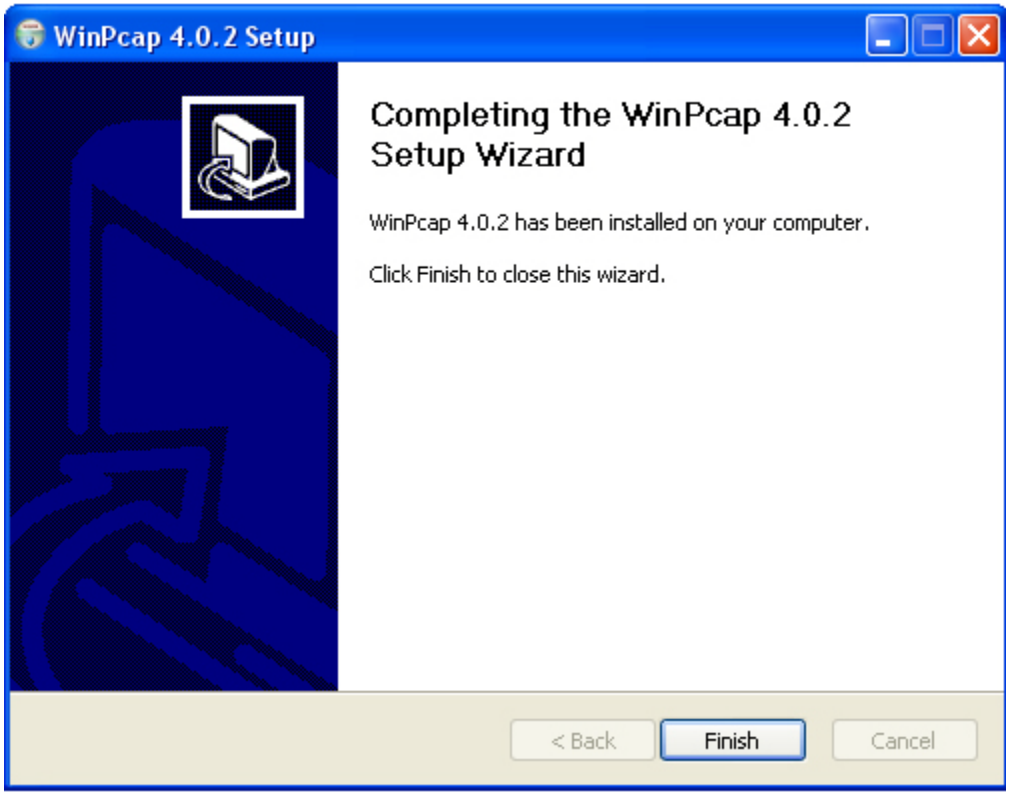


Figure 1-52: **WinPcap Installation Wizard Successful**

Click **Finish**.

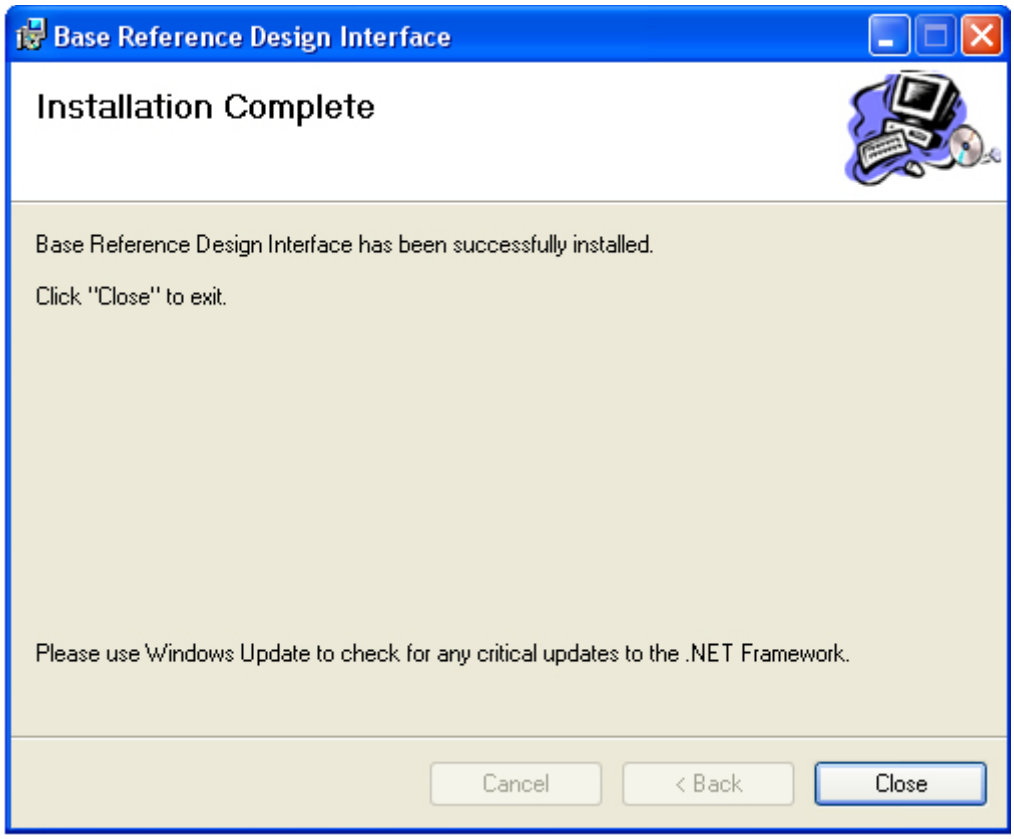


Figure 1-53: **BRD Installation Complete**

Click **Close**.

Running the Base Reference Design

Now that you have the ML605 set up and the Base Reference Design Application software installed, you can run the demo. You should have the Ethernet cable connected between the ML605 board and your PC Ethernet port.

Note: Turn off any wireless cards while running this demonstration.

To start the application GUI, please go to your Windows START menu and select **All Programs → XILINX → Base Reference Design → Base Reference Design Interface**

The GUI shown in Figure 1-54 will start.

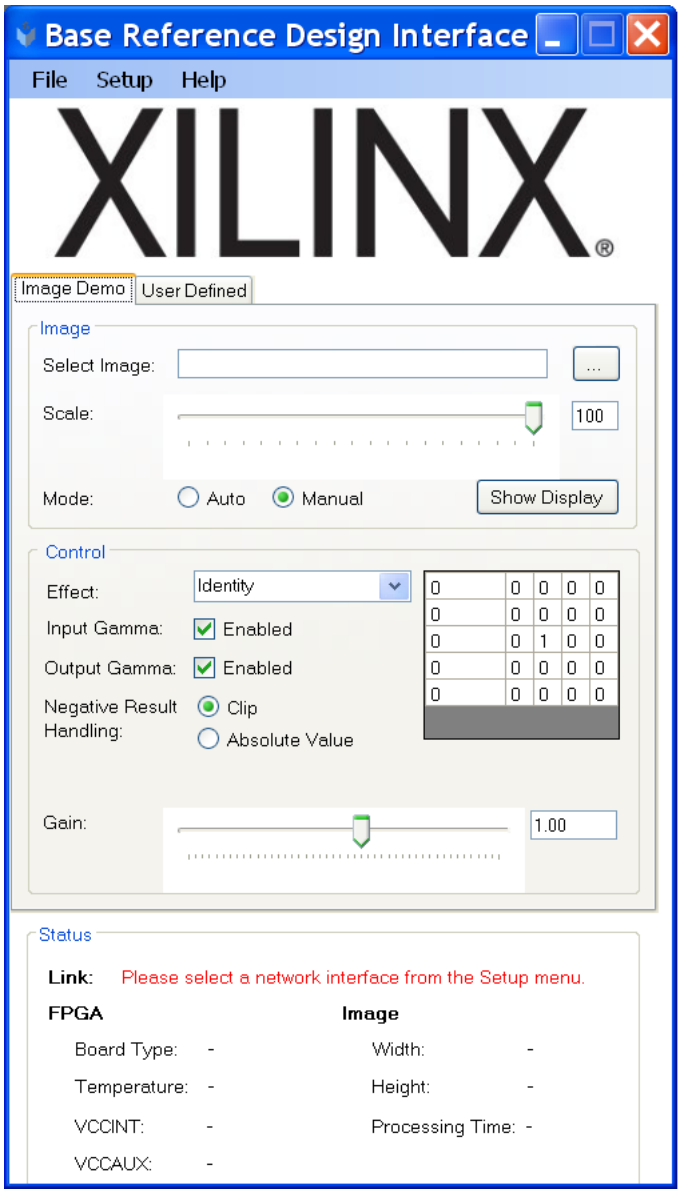


Figure 1-54: **Network Link Setup Request**

You will notice in the Status field at the bottom of the GUI that the Link needs to be set.

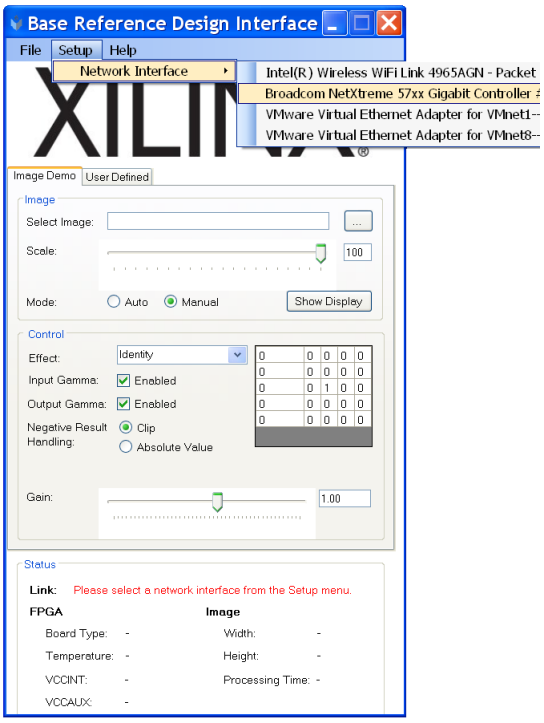


Figure 1-55: **Setup Network Interface Connected to ML605**

Select the menu item Setup, then select the appropriate Wired Network. Wait for few seconds and then press SW3 on the ML605 to configure the FPGA using the System ACE CF controller and the CompactFlash card.

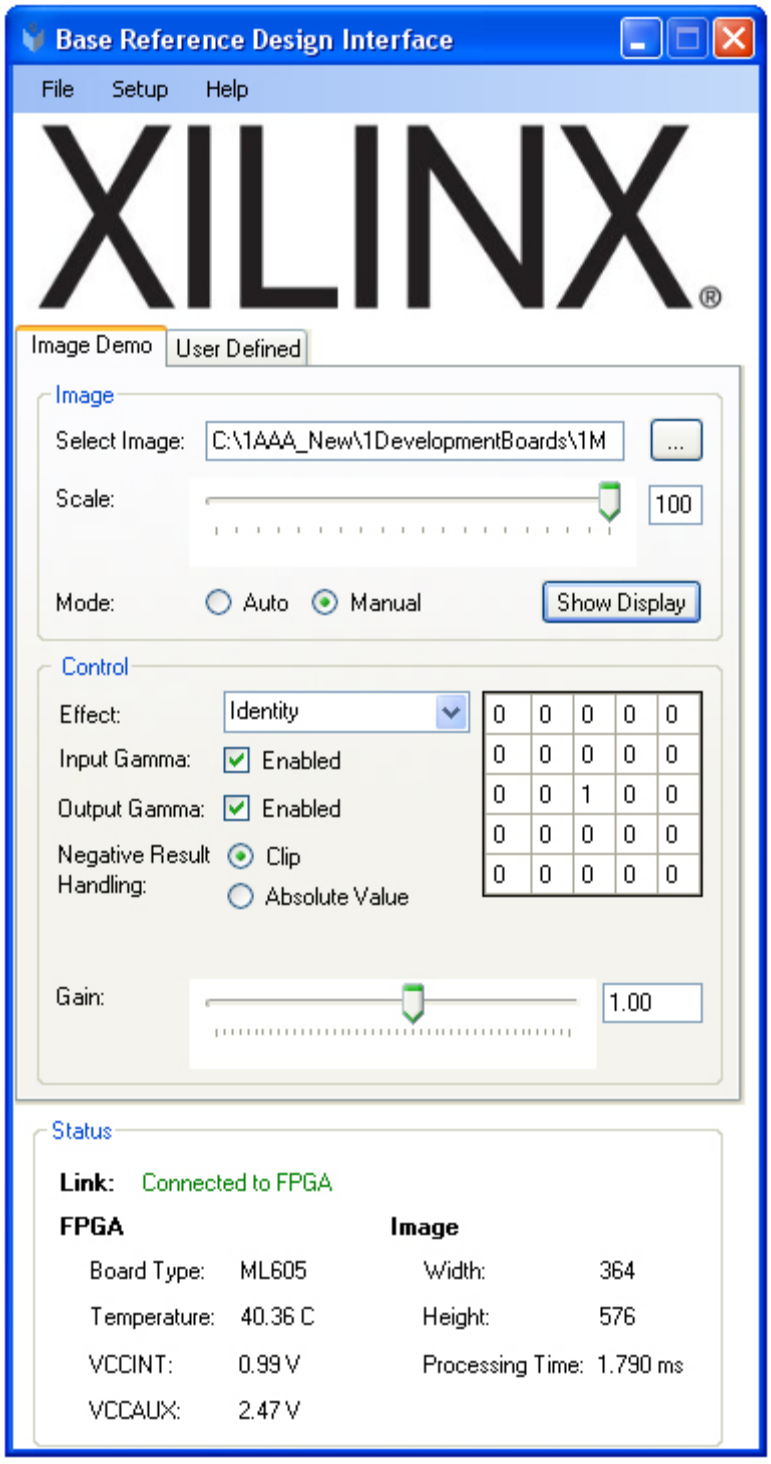


Figure 1-56: **Successfully Connected to ML605**

You can now select an image. It is best to select an image smaller than 1024 pixels wide. On the USB flash drive there are a number of images to select or you can select one of your

own images. To select one of the provided images, look in the ML605_BRD _Images directory.

In the Image section of the GUI, use the browse button to navigate to an image. After you have selected the image, click the Show Display button. This will display two side-by-side images. The leftmost image is the unaltered image, and the rightmost image is the image that has been filtered by the FPGA. Unless the effect has been changed, the default effect is Identity (Figure 1-57).

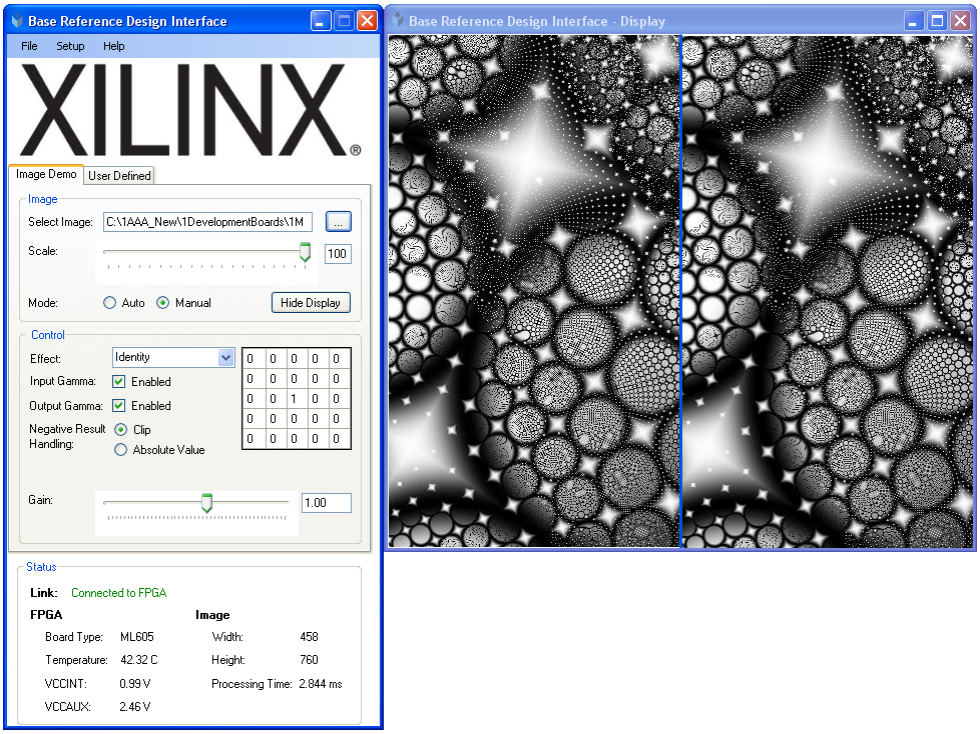


Figure 1-57: **Original and FPGA Filtered Images using Identity Effect**

Using the pull-down menu, select a different effect. For example, select SobelX. The filtering transform will display. As you can see in Figure 1-58, the image is updated using the selected filter operation.

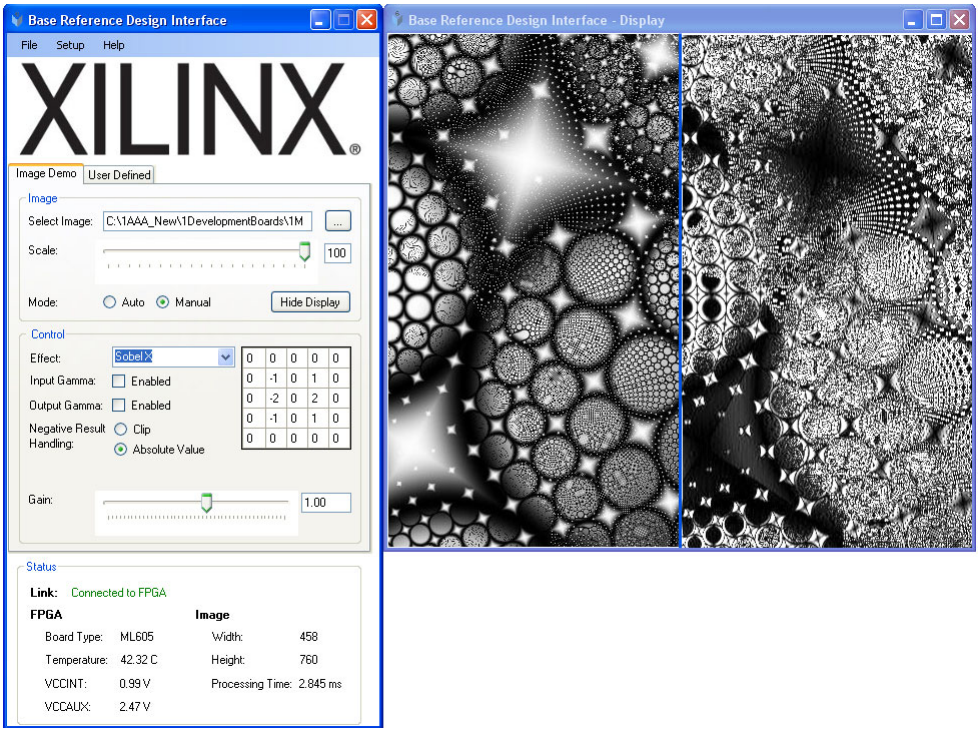


Figure 1-58: **Original and FPGA Filtered Images using SobelX Effect**

Select **Smooth effect** and notice how the 2-D FIR filter coefficient matrix values change. Figure 1-59 shows how the image display changes as well.

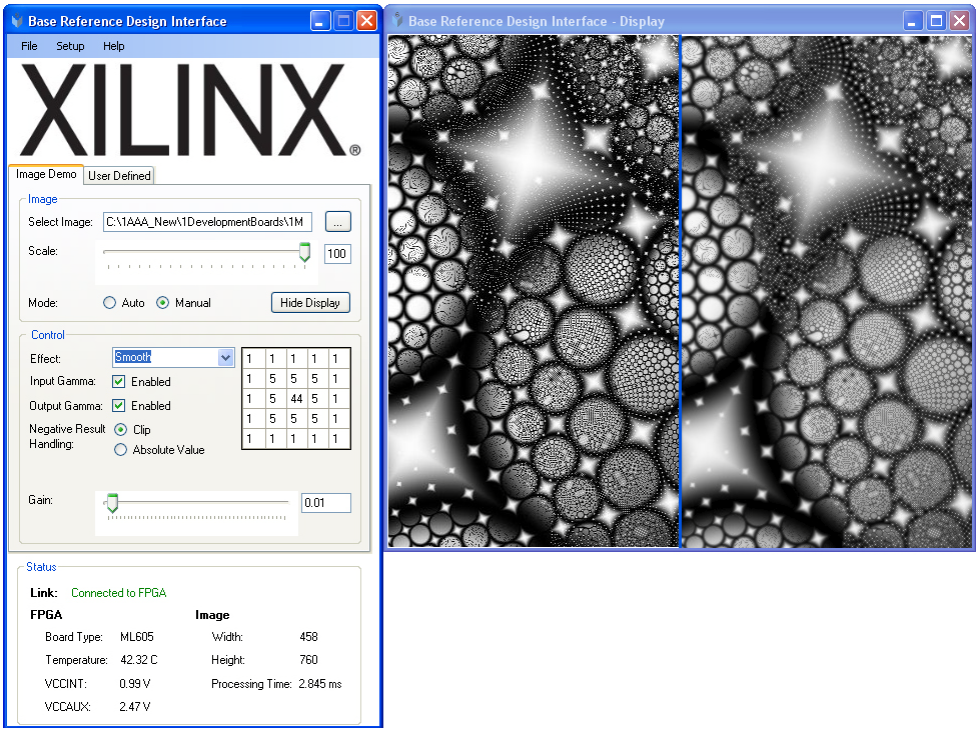


Figure 1-59: **Original and FPGA Filtered Images using Smooth Effect**

Choose Edge Detect from the effect menu. The filtering transform shown in Figure 1-60 will be displayed.

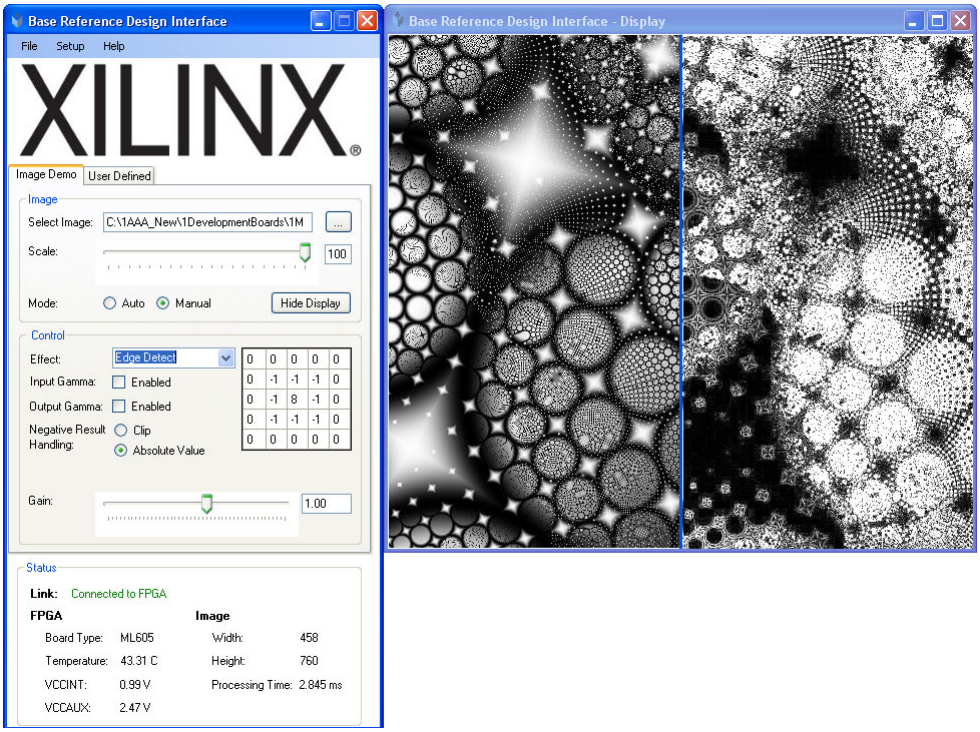


Figure 1-60: **Original and FPGA Filtered Images using Edge Detect Effect**

Different effects can be set automatically by selecting the **Auto** mode button.

FPGA temperature, VCCINT, VCCAUX, Image dimensions, and processing time are also reported by the Status field.

You have now completed running the reference design.

Installing the ISE Software

The ML605 evaluation kit includes entitlement to a seat that permits the ISE Design Suite: Logic Edition to be used with a Virtex-6 XC6VLX240T-1FFG1156C FPGA. This software can be installed from the DVD provided with the kit. The latest version can also be downloaded from http://www.xilinx.com/support/download/index.htm.

The ML605 evaluation kit also works with the software listed here:

- ISE Design Suite: Embedded Edition
- ISE Design Suite: DSP Edition
- ISE Design Suite: System Edition

Update the software before working with the evaluation kit. Updates can be downloaded from http://www.xilinx.com/support/download/index.htm

To install the ISE Design Suite: Logic Edition software from the DVD included with the ML605 evaluation kit:

1. Activate the software license. See "Redeeming the Software and IP License."

2. Insert the DVD provided with the ML605 kit in the host computer's drive.
3. Follow the instructions provided by the installation software.

Redeeming the Software and IP License

A software voucher similar to the example shown in Figure 1-61 is included with each ML605 evaluation kit. The voucher contains the code that is used to create a device-locked software license for the ISE software and/or the IP included with the evaluation kit.

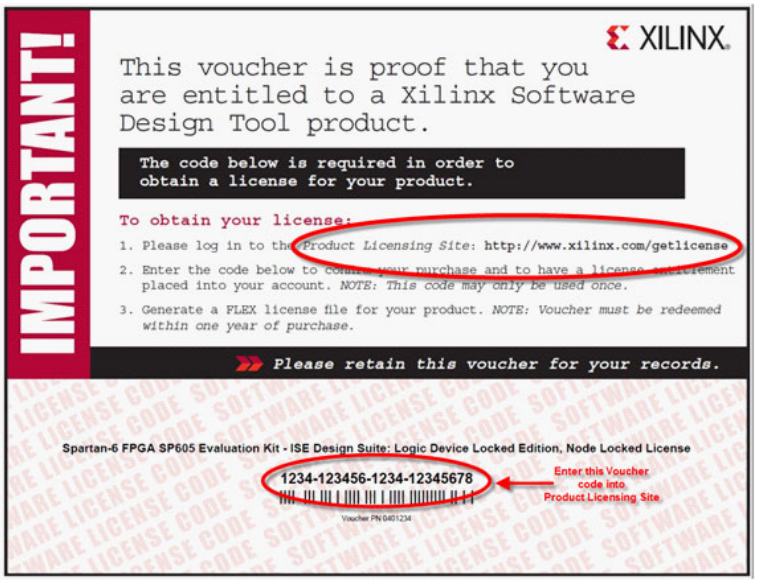


Figure 1-61: **Software Voucher**

To create a license:

1. Go to www.xilinx.com/getlicense/ (Figure 1-62).

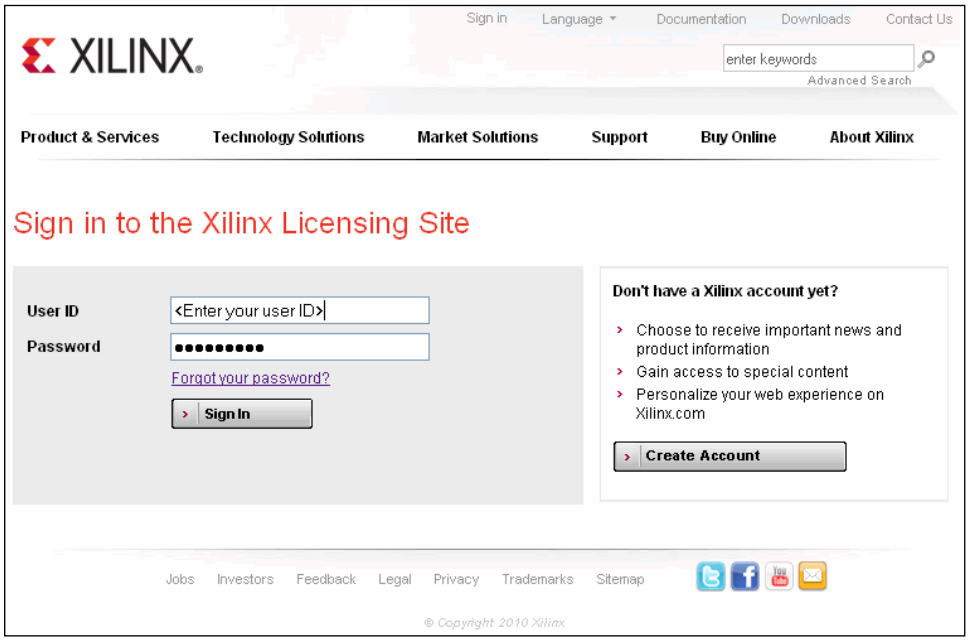


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Figure 1-62: **Licensing Site Sign-In Page**

2. If you have a Xilinx account, enter your **User ID**, **Password** and click **Sign In**. If you don't have an account, click **Create Account** to create one.

   Note: If you have questions or need help, contact Xilinx customer service at: http://www.xilinx.com/support/techsup/tappinfo.htm.

3. After signing in, confirm your contact information is correct and click **Next**.
4. Under the **Create New Licenses** tab, enter the 22-digit code from the voucher in the field shown in Figure 1-63. Click **Redeem Now**.

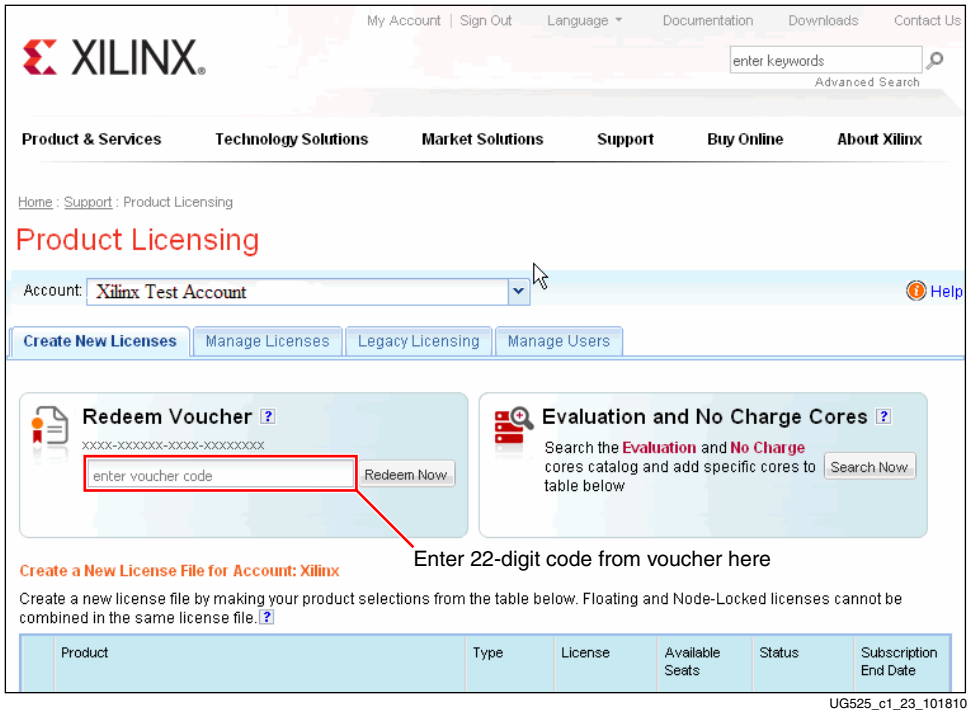


Figure 1-63: **Redeem Voucher**

The software represented by the voucher code is added to the product table and is selected (checked) for licensing as shown in Figure 1-64.

Note: The software descriptions shown in Figure 1-64 are examples and might differ from the descriptions shown on the actual page.

5. Click **Generate Node Locked License** at the bottom of the page to start the license generation flow (Figure 1-64).

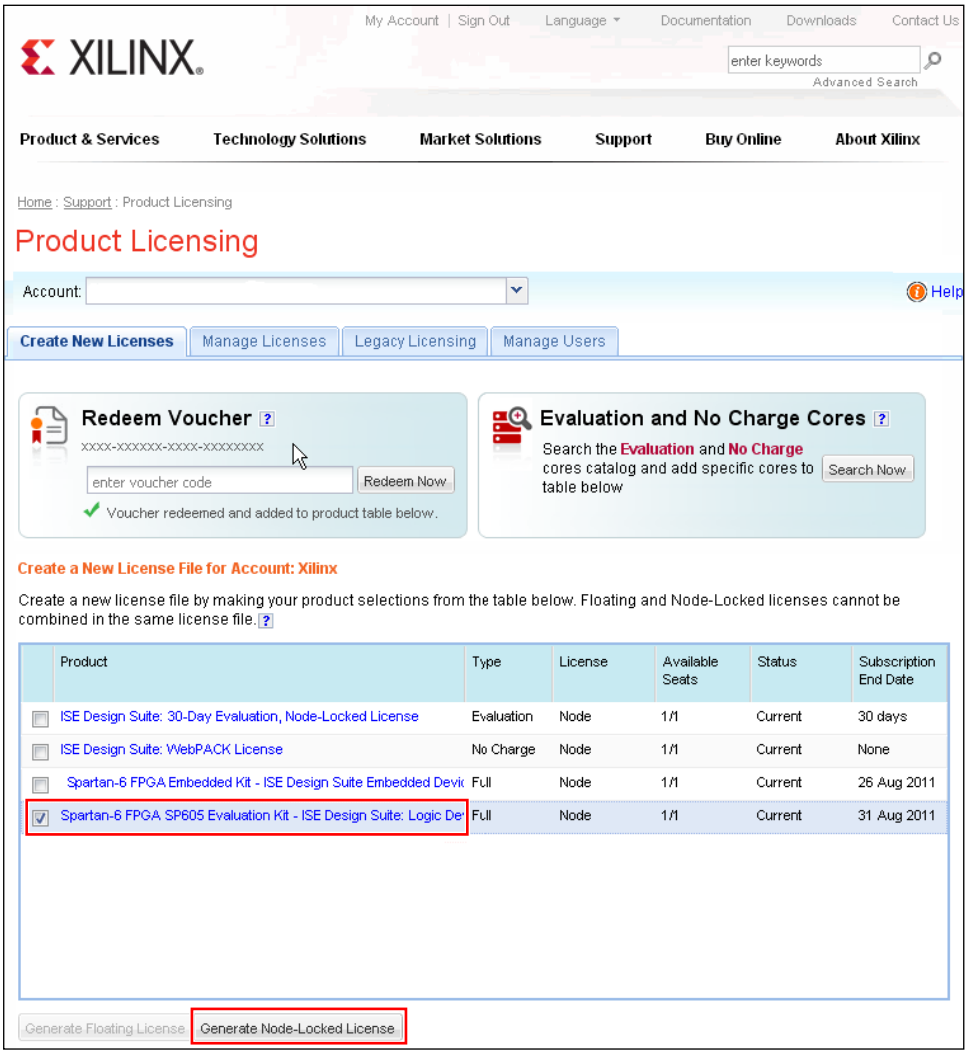
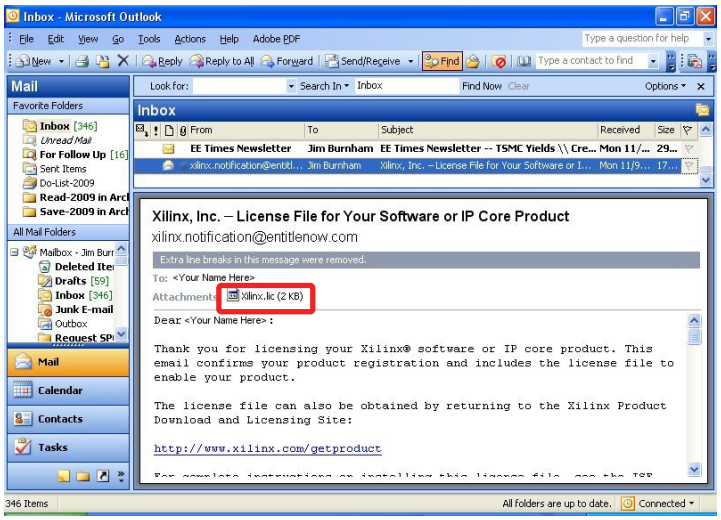


Figure 1-64: **Generate License**

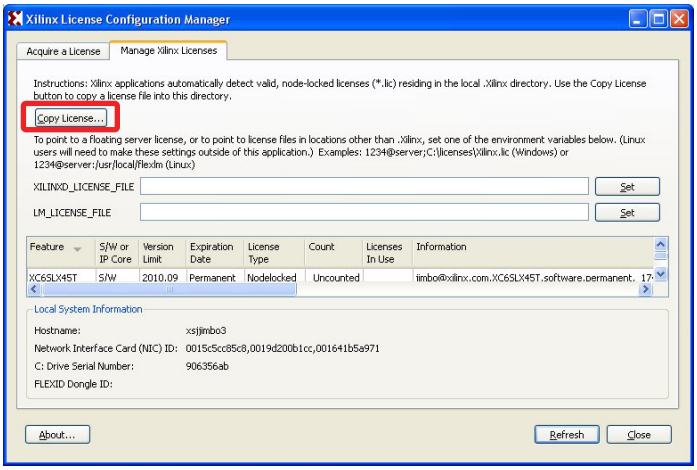
6. When prompted to select a host name for the license, select a host ID. The host ID can be a dongle serial number, Ethernet MAC address, or a disk volume ID.
7. When license generation is complete, the license will be emailed to you. Follow the instructions in the Xilinx License email to complete the licensing process (Figure 1-65).



UG525_35_111209

Figure 1-65: **Xilinx License Notification E-mail**

8. Go back to the Xilinx License Configuration Manager dialog and click **Copy License...** (Figure 1-66).



UG525_36_111209

Figure 1-66: **Manage Xilinx License Tab**

9. Navigate to the location where the `Xilinx.lic` file is saved and select it (Figure 1-67).

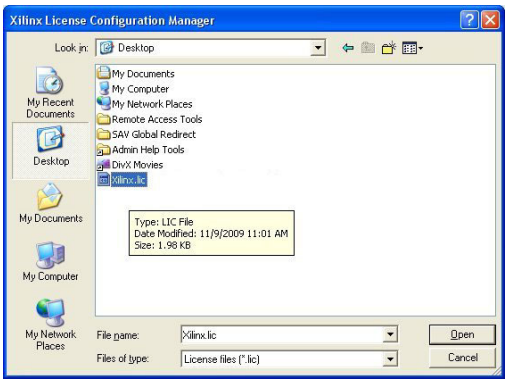
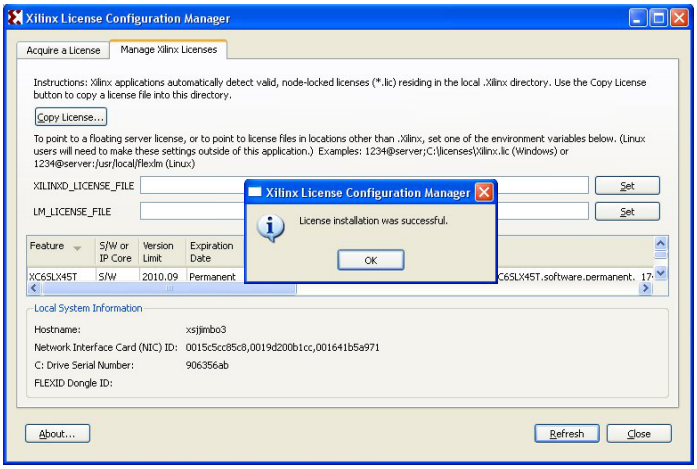


Figure 1-67: **Select the `Xilinx.lic` file**

The ISE software license is now installed. Click **OK** on the Success Dialog (Figure 1-68) to close the Xilinx License Configuration Manager.



UG525_38_111209

Figure 1-68: **License Installation Successful**

Now What?

After following the steps in this Getting Started Guide, you can test the features of the board using the ML605 Board Diagnostic Flash and PCI Express demonstrations. You now have a complete and updated installation of the Xilinx ISE Device-Locked to Virtex-6 LX240T FPGA software, and should have been able to open your first project.

Additional resources are located on the ML605 product page at http://www.xilinx.com/ml605. You are encouraged to check the ML605 Evaluation Kit home page regularly for the latest in documentation, FAQs, reference design examples, product updates, and known issues.

Getting Additional Help and Support

Support

For questions regarding products within your Product Entitlement Account or if you feel you have received this notification in error, send an email message to your regional Customer Service Representative:

Canada, USA and South America - isscs_cases@xilinx.com

Europe, Middle East, and Africa - eucases@xilinx.com

Asia Pacific including Japan - apaccase@xilinx.com

For technical support including the installation and use of your product license file you may contact Xilinx Online Technical Support at www.support.xilinx.com. On this site you will also find the following resources for assistance:

Software, IP and Documentation Updates

Access to Technical Support Web Tools

Searchable Answer Database with Over 4,000 Solutions

User Forums

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Appendix A

References

This section provides references to documentation supporting Virtex-6 FPGAs, tools, and IP. For additional information, see www.xilinx.com/support/documentation/index.htm.

1. UG534, *ML605 Hardware User Guide*
2. UG535, *ML605 Reference Design User Guide*
3. DS150, *Virtex-6 Family Overview*
4. DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*
5. UG360, *Virtex-6 FPGA Configuration User Guide*
6. UG361, *Virtex-6 FPGA SelectIO Resources User Guide*
7. UG362, *Virtex-6 FPGA User Guide: Clocking Resources*
8. UG363, *Virtex-6 FPGA Memory Resources User Guide*
9. UG364, *Virtex-6 FPGA Configurable Logic Block User Guide*
10. UG365, *Virtex-6 FPGA Packaging and Pinout Specifications*
11. UG366, *Virtex-6 FPGA GTX Transceivers User Guide*
12. UG369, *Virtex-6 FPGA DSP48E1 Slice User Guide*
13. DS186, *Virtex-6 FPGA Memory Interface Solutions Data Sheet*
14. UG370, *Virtex-6 FPGA System Monitor User Guide*
15. DS643, *Multi-Port Memory Controller (MPMC) (v5.02a) Data Sheet*
16. UG086, *Memory Interface Solutions User Guide*
17. UG138, *LogiCORE™ IP Tri-Mode Ethernet MAC v4.3 User Guide*
18. UG517, *LogiCORE™ IP Virtex-6 FPGA Integrated Block User Guide v1.3 for PCI Express*
19. DS715, *Virtex-6 FPGA Integrated Block v1.3 for PCI Express Data Sheet*
20. Platform Studio EDK

ML605 tutorials and design files are located at http://www.xilinx.com/products/boards/ml605/reference_designs.htm:

21. *ML605 Built-In Self Test Flash Application*
22. *ML605 MIG Design Creation*
23. *ML605 PCIe x8 Gen1 Design Creation*
24. *ML605 PCIe x4 Gen2 Design Creation*
25. *ML605 MultiBoot Design*
26. *ML605 GTX IBERT Design Creation*
27. *ML605 System Monitor*
28. *ML605 Restoring Flash Contents*