Data Format UFO 5

The data format has been changed in order to improve the performance of the architecture for on-line data elaboration like back-ground on-line subtraction.

The HEADER has some structure that previous version

Example:

0x51111111 0x52222222 0x53333333 0x54444444
0x55555555 0x50000440 0x55000000 0x50000000

Description:

DHEADER_1 = {4'h5, 28'h1111111};
DHEADER_2 = {4'h5, 28'h2222222};
DHEADER_3 = {4'h5, 28'h3333333};
DHEADER_4 = {4'h5, 28'h4444444};
DHEADER_5 = {4'h5, 28'h5555555};
DHEADER_6 = {4'h5, CMOSIS_start_addr[9:0], skip_lines[6:0], number_of_lines};
DHEADER_7 = {4'h5, 4'h5, frame_number}; → already for vers. 5

New field for 10-12 bits in HEADER_8

DHEADER_8 = {4'h5, ADC_Resolution, Output_mode, FR_timestap};

ADC_Resolution, Output_mode → both 2 bits wide

ADC Resolution	ADC_Resolution (code)
10 –bit	0
11 –bit	1
12 –bit	2
Output_mode	**Code**
16 outputs (used)	0
8 outputs (not used)	1
4 outputs (used)	2
2 outputs (not used)	3

The TAIL has some structure that previous version

Example:

0x0aaaaaaa 0x840dffff 0x0f001001 0x28000111
0x2xxxxx 0x0xxxxx 0x00000000 0x01111111

Description:

TAIL_1 = {4'h0, 28'hAAAAAAA};

TAIL_2 = status1;
TAIL_3 = status2;
TAIL_4 = status3;
TAIL_5 = {4'h0, 2'h0, app_addr_rd};
TAIL_6 {4'h0, 2'h0, app_addr_wr};
TAIL_7 = {4'h0, 28'h0000000};
TAIL_8 = {4'h0, 28'h1111111};

Where the status bit are:
status1 = {1'b1, 1'b0, FSM_Master_Ctrl, status_bit_int_CMOSIS_IN[25:0]}; status2 = {3'b0, end_of_all_FR, error_status, rd_data_count_fifo_255_64, full_FIFO_255_64, empty_FIFO_255_64, 2'b0, wr_data_count_fifo_DATA_to_DDR, full_FIFO_data_to_DDR, empty_FIFO_Data_to_DDR};

status3 = {2'b0, BUSY_status, error_desc_1, 1'b0, FSM_RD_DDR3, 1'b0, FSM_WR_DDR3, 1'b0, FSM_ARBITER_DDR3};

The payload packet size is 256 bits, each packet contain 256 bits organized as shown below:

Header	00000000	00000000	Pix col 0..				Pix col 15
32 bit	32 bit	32 bit	⟷				
			160 bit				

Example:
0x80a00000 0x00000000 0x00000000 0x595794d9
0xd96c5257 0x6d5655e5 0x97059571 0xf5a96b59
N.B. The 32 bit gap is a flexible gap to preserve space for 12 or more bit/pixel. The header above must be considered for 10bits per pixel.

Where Header is:
header = {10000000, pixel_size_reg(4 bit), 0,row_number_reg (11 bit) ,0, pixel_number_reg(7) };
Pixel number → from 0 to 127
Row_number → configurable but default from 0 to 1088

Pixel organization

Pix0	..	Pix0		Pix0		Pix0	..	..	Pix0

Output 0 Output 1 Output 2 Output 15

12 bit version

For 12-bit mode the Header is :
0x80c00000 0xa18317f118517517 0x18b18f188618718b 0x8e19018831801731
Where 0x80c00000 contains same field describe for 10-bit and the c → indicate 12 –bit.

The data are sent like 12-bit mode but must be sample with 12-bit width.

Header	00000000	Pix col 0..	Pix col 0..				Pix col 15
32 bit	32 bit	←					→
		192 bit					

Example:
0x80c00172 0x718f18911a318b19 0x1a21b5199c19f1a2 0x9b1a0181f1991a11

The control word in the tail is present at the end of each row:
0xc0c0007f 0x5055055005505505 0x550550555055055 0x5505505550550550 (only for the first row)
xc0c00100 0x5055055005505505 0x550550555055055 0x5505505550550550 (others rows)

Example:

0x80c00172 0x718f18911a318b19 0x1a21b5199c19f1a2 0x9b1a0181f1991a11
0x80c00173 0x11a01a811911841a 0x19d19e19a71a81a0 0xa019d19be1a11941
0x80c00174 0x91a31a0119019a1a 0x1a21a21a9a1ac19d 0xad19819cf1a11ac1
0x80c00175 0xe19e1aa118419c19 0x1a619e1a9d1a41a3 0xa41a218d01aa1981
0x80c00176 0xc19a19f118519919 0x19819b1ba119f1a6 0xad1a119201901a11
0x80c00177 0xe195190118118718 0x1a319d1aa7199196 0xa11a0196319c1a11
0x80c00178 0x619018d118419a19 0x1a81aa1a951a21a1 0xa41b3193e19719a1
0x80c00179 0x19b1a1118d18719 0x1941a11aab1991a7 0xac1931a761a119a1
0x80c0017a 0x4197192118d1a419 0x1891a21aaa19319e 0xa31a719051921a21
0x80c0017b 0xb19519f119919219 0x19e1a61aa21951a3 0x9d1ae189618e1ac1
0x80c0017c 0xc18d19e119c19b19 0x19a19719b0199197 0x9e1a319fe1a71a31
0x80c0017d 0x61931ad119b18c18 0x19119f1a991a4196 0x9e19619c81a918d1
0x80c0017e 0xa1a01a7119818d19 0x19f1a2199619519f 0xa419418bc1ab1a01
0x80c0017f 0xd1941ae119318e19 0x19e19f1a911a419b 0x98195196d19b1a01 → last 256-bit of the row
0xc0c00100 0x5055055005505505 0x550550555055055 0x5505505550550550 → row tail

Bank Register for Camera + FPGA Control & Status

New bank register organization compatible with the previous version, following you can find the registers address and description. This is the output available when the ./Status.sh is executed.

Bank Reg. example:

Status ...

fe409000: 0000c800 00000000 0000c800 00000000
fe409010: 000bc800 00000000 000bc800 00000000
fe409020: 00000004 00000000 00000004 00000000
fe409030: 00000005 00000000 00000005 00000000
fe409040: 00000201 00000000 00000201 00000000
fe409050: 8449ffff 0f001001 3ffff111 00000000
fe409060: 00000000 00000000 00000000 00000000
fe409070: 00089108 0011220c 00112210 00000000
fe409080: 00000000 00000000 00000000 00000000
fe409090: 00000000 00000000 00000000 00000000
fe4090a0: 00000000 00000000 00000000 00000000
fe4090b0: 00000000 00000000 00000000 00000000
fe4090c0: 00000000 00000000 00000000 00000000
fe4090d0: 00000000 00000000 00000000 00000000
fe4090e0: 00000000 00000000 00000000 00000000
fe4090f0: 00000000 00000000 00000000 00000000
fe409100: 00001000 00000000 00000000 00000000
fe409110: 14830466 00000000 14830466 00000000
fe409120: 00000440 00000000 00000440 00000000
fe409130: 00000000 00000000 00000000 00000000
fe409140: 00000025 00000000 00000025 00000000
fe409150: 02800000 00000000 02800000 00000000
fe409160: 00000000 00000000 00000000 00000000
fe409170: 00000080 00000000 00000080 00000000
fe409180: 00000280 00000000 00000280 00000000
fe409190: 07735940 00000000 07735940 00000000
fe4091a0: 00000064 00000000 00000000 00000000
fe4091b0: 00000000 00000000 00000000 00000000

Address	Like	description
9000	0000c800	To configure the CMOSIS param.
9010	000bc800	Feedback after the writing. The MSB code → b → If no error are present
9020	00000004	SPI speed grade → do not care
9030	00000005	{12'b0, 2'b0, Output_mode, 2'b0, ADC_Resolution, 3'b0,bit_mode, ReadFirmware_Ver}; *
9040	00000201	Control register → see excel file
9050	8449ffff 0f001001 3ffff111 00000000	Status 1 Status 2 Status 3 → will be Fast Reject status For bit description see the excel file

9070	00089108 0011220c 00112210 00000000	DDR Memory pointer in Start DDR_ ADDRESS END_DDR_ADDRESS RD_DDR_ADDRESS Do not care
90a0	CMOSIS_PARAM_1	9:0 skip_num_of_lines_in, 10:20 num_of_lines_CMOSIS, 21:31 start CMOSIS address
90b0	CMOSIS_PARAM_2	10:0 CMOSIS threshold line (for Fast Reject mode)
90c0	SKIPE_LINES	For Uros like a threshold when the camera is in interleaving mode
9100	00001000	RAWDATA_PKT_ADDR
9110	14830466	[2:0] FPGA_Monitor_temp_allarms, [9:0]fpga_temperature, sensor_temp[18:0] **
9120	00000440	Number of rows (readout)
9130	START_POS_ADD	First ROW in the readout (Start row position)
9140	00000025	EXP_TIME_EXT
9150	02800000	GAIN_AND_MOTOR_POS_ADD → {4'h0, ADC_gain_reg, Motor_X_reg, Motor_Y_reg, Motor_Z_reg, Phi_deg_reg}; ***
9010	000bc800	Feedback after the writing. The MSB code → b → If no error are present
9170	00000080	NUMBER_OF_TRIGGERS→ this set the number of frames when the stimuli.sh is used
9180	00000280	TRIGGER_PERIOD → set the frame rate in FPGA (min value is 0x280)
9190	07735940	Sample period of the CMOSIS temperature → do not care
91a0	00000064	Max number of frame in the DDR, works like threshold, if the number of frame in DDR is = at this threshold the Busy is ON
91b0	00000000	Number of frame in DDR - Number of frame sent by DMA. Give you the number of frame still not trasmitted

* Output_mode = ADC_Resolution → 2 bits. bit_mode → 1bit . ReadFirmware_Ver → 8 bits

** FPGA_Monitor_temp_allarms → must be always 0x0

*** ADC_gain_reg → 8 bits. Motor_X_reg= Motor_Y_reg= Motor_Z_reg=Phi_deg_reg →5 bits