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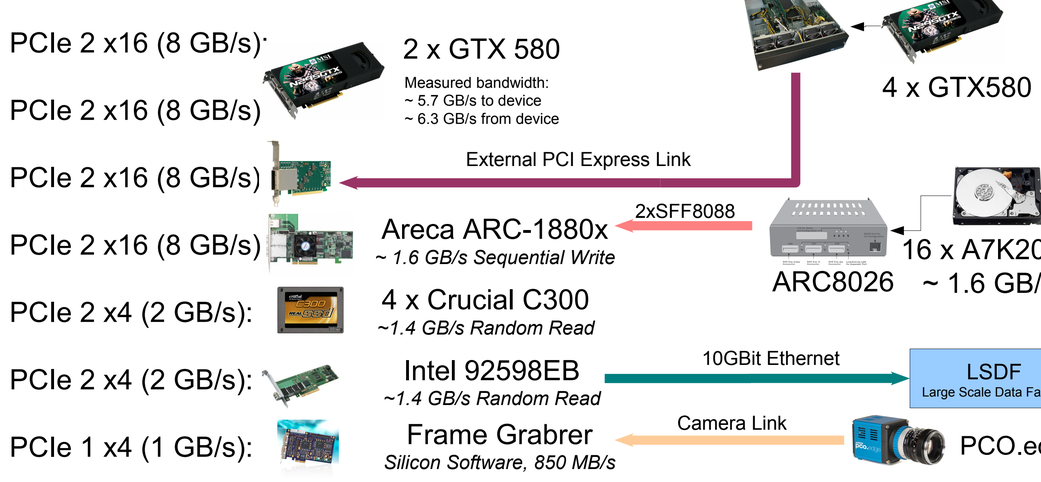
Assessment at Synchrotron Experiments

A. Kopmann[1], A. Mirone[2], T. dos Santos Rolo[1]

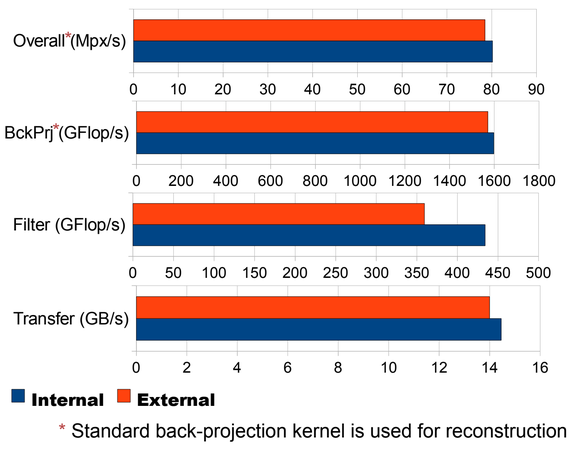
[2] *European Synchrotron Radiation Facility, Grenoble, France*

Imaging Station

SuperMicro 7046GT-TRF (Dual Intel 5520 Chipset)
CPU: 2 x Xeon X5650 (total 12 cores at 2.66 Ghz)
GPUs: 2 x GTX 580 + 4 x GTX580 External
Memory: 96 GB / 12 DDR3 slots (192GB max)



External GPU Box



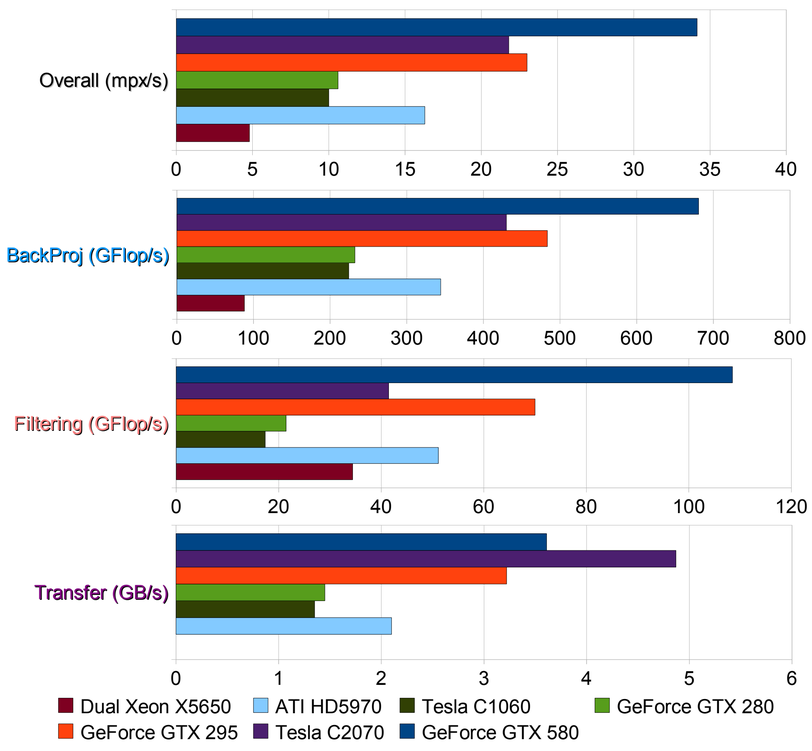
* Standard back-projection kernel is used for reconstruction

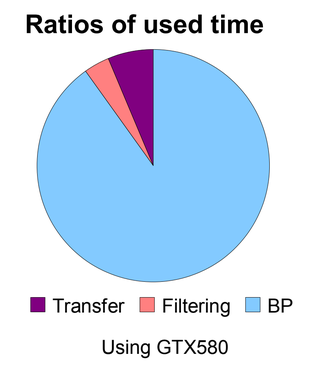
Performance of 4 GTX580 cards connected internally or in the external box sharing a single PCIe x16 link using PLX PEX8648 switch.

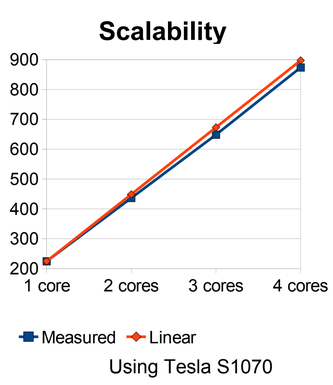
GPU Evaluation

	GTX580	Tesla C2070	GTX295	GTX280	Tesla C1060	ATI HD5970*	Xeon X5650
Architecture	Fermi	Fermi	GT200	GT200	GT200	Cypress	Nehalem
Processors	1 x 512 1.54 GHz	1 x 448 1.15GHz	2 x 240 1.3 GHz	1 x 240 1.3 GHz	1 x 240 1.25 GHz	2 x 1600 0.725 GHz	2 x 6 2.66 GHz
Theoret. SP	1.58 TFlops	1.03 TFlops	1.79 TFlops	0.93 TFlops	0.62 TFlops	4.64 TFlops	0.13 TFlops
Theoret. DP	0.20 TFlops	0.51 TFlops	0.15 TFlops	0.08 TFlops	0.07 TFlops	0.93 TFlops	0.06 TFlops
Memory	1.5 GB 192 GB/s	6GB 144 GB/s	2 x 900 MB 112 GB/s	1 GB 142 GB/s	4 GB 102 GB/s	2 x 0.5 GB 128 GB/s	96 GB 32 GB/s
Texture	1 x 49.4 GT/s	1 x 42 GT/s	2 x 46 GT/s	1 x 48 GT/s	1 x 48 GT/s	2 x 58 GT/s	
Power Cons.	244 W	238 W	289 W	236 W	188 W	294 W	2 x 95 W
Software	CUDA 3.2	CUDA 3.2	CUDA 3.2	CUDA 3.2	CUDA 3.2	APPSDK 2.5	glibc 2.11.2
Driver	270.41.19	270.41.19	270.41.19	270.41.19	270.41.19	11.10	2.6.37

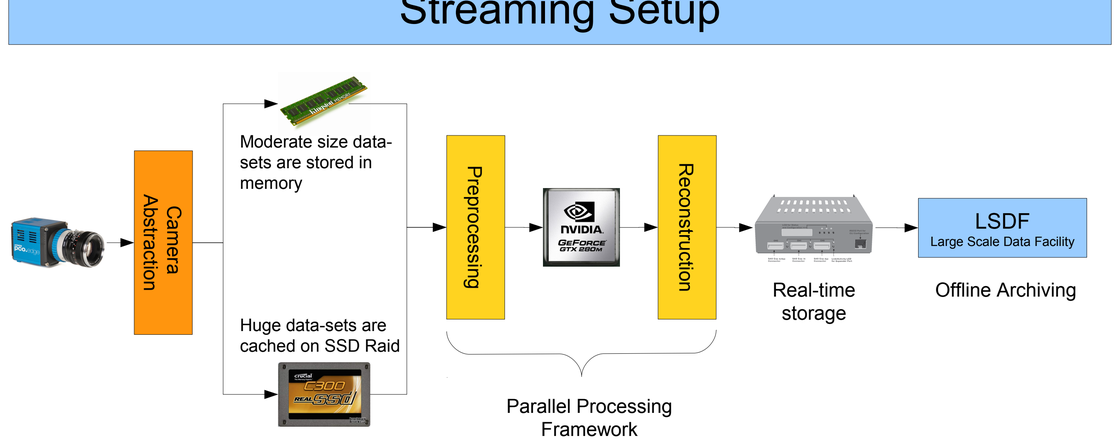
* With HD5970 currently it is possible to use a single core only







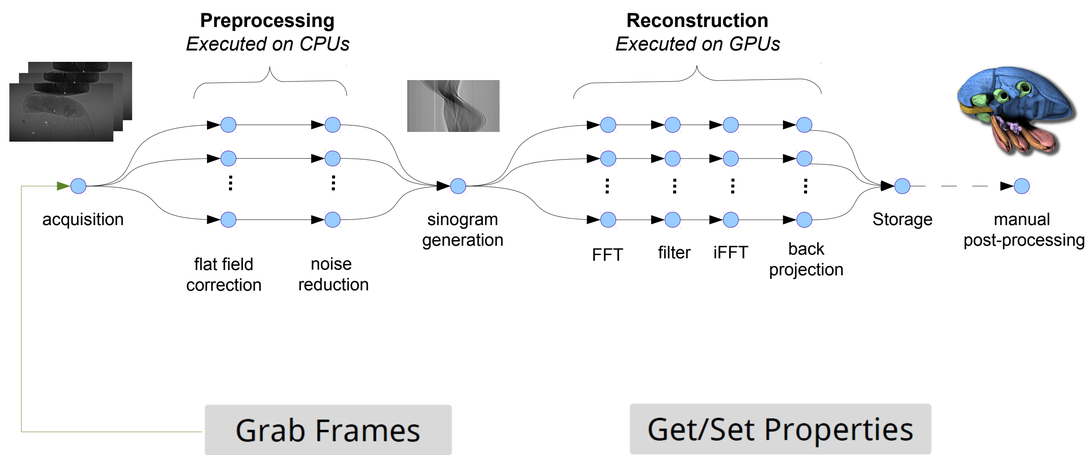
Streaming Setup

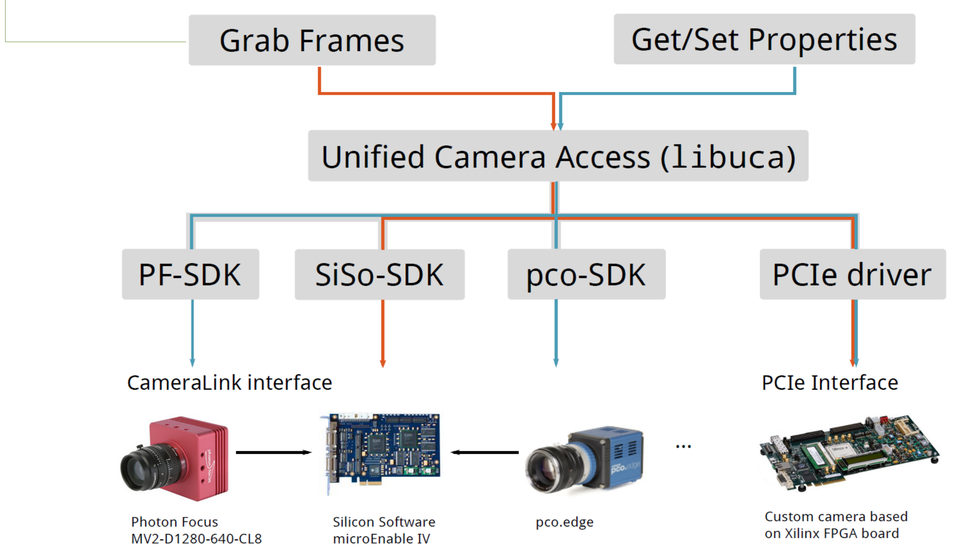


Parallel Processing Framework

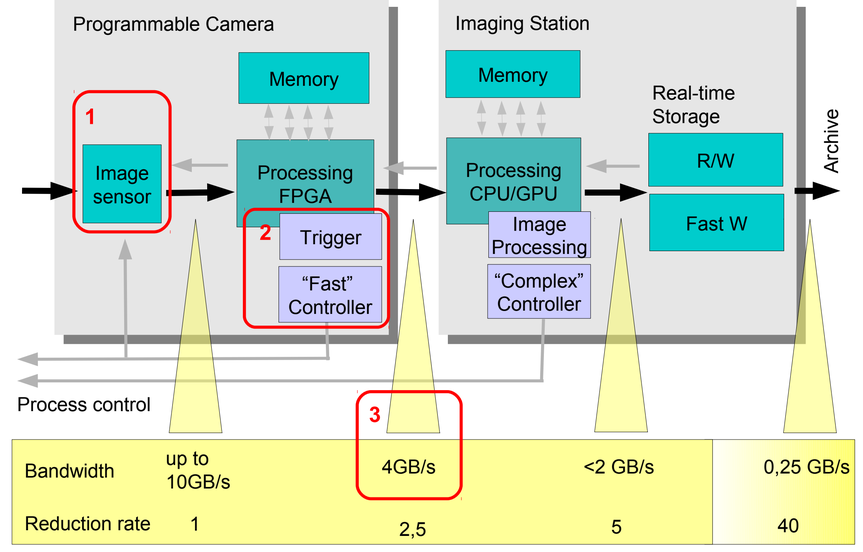
Camera Abstraction
- Frame-grabbing & configuration interfaces
- CameraLink, Firewire, PCI-express cameras
- Synchronous & asynchronous modes

Parallel Processing Framework
- Stream processing using pipelines of filter nodes
- Hardware-aware scheduling
- Bindings to scripting languages (python, etc.)





Vision



Fast image processing is key for the advanced features like image-based process control, image-content based triggers depending on sample dynamics, as well as autonomous optimization of beam properties. To facilitate image-based control, we develop a programmable high-speed camera. Highlights of the programmable camera are its modular design with a replaceable image sensor (1), application specific camera-side trigger, compression and control algorithms (2) and the high-speed interface to the compute server (3). The modular design ensures fast adoption to future generations of image sensors and bus standards. We aim to reach a camera readout bandwidth of up to 4GB/sec.

Suren Chilingaryan <Suren.Chilingaryan@kit.edu>
Matthias Vogelgesang <Matthias.Vogelgesang@kit.edu>

Project Documentation & Sources
http:///ufo.kit.edu/pyhst/