Karlsruhe Institute of Technology

IPE camera
Hardware & Software Status

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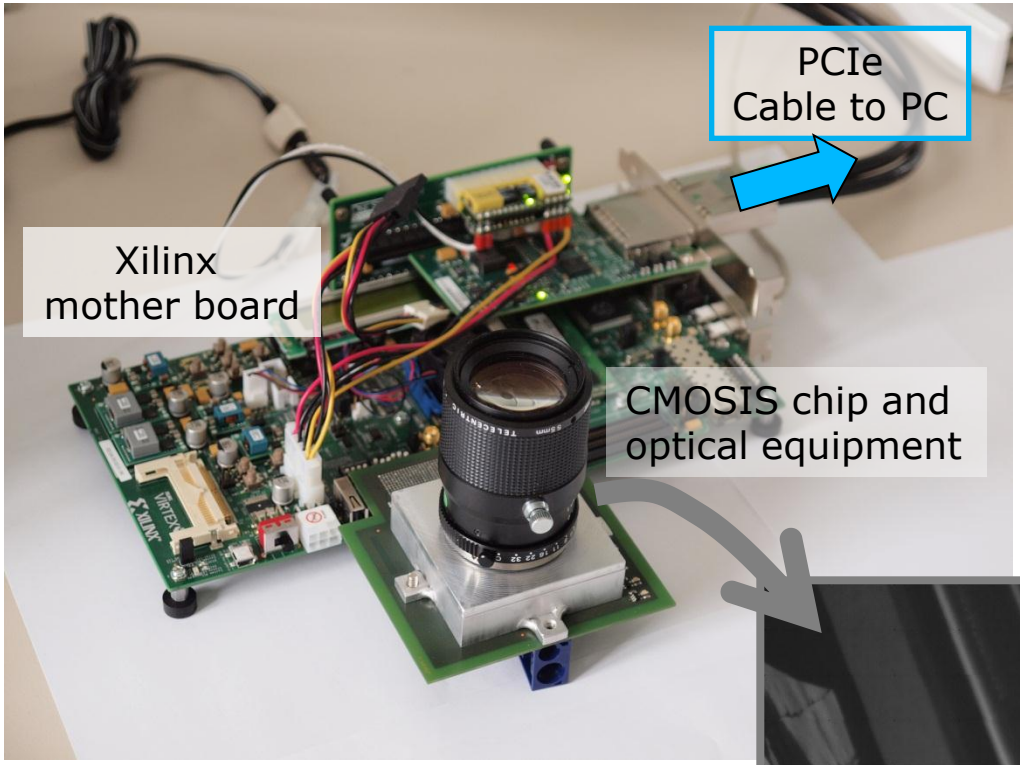
Outline

- FPGA readout architecture → overview and status
- HW and SW integration → overview and status
- What's next

→ see Uros's talk → IPE camera tuning and temperature control system

UFO Overview



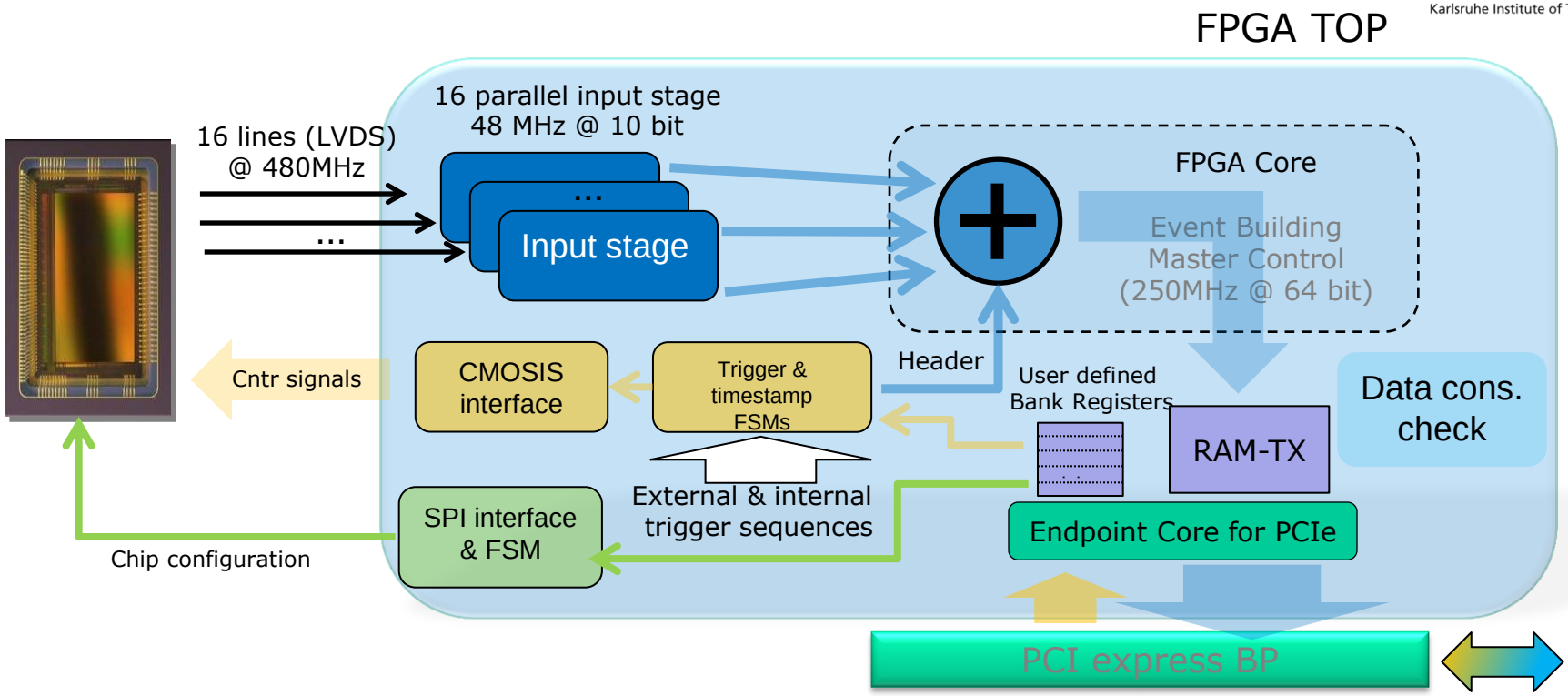
In the last 3 months:

- HW – Firmware develop.
- HW debug (mezzanine board)
- Software develop. (driver+GUI)
- Cooling system "proto" → details in Uros's talk
- Mechanical support

→ Camera fully operational

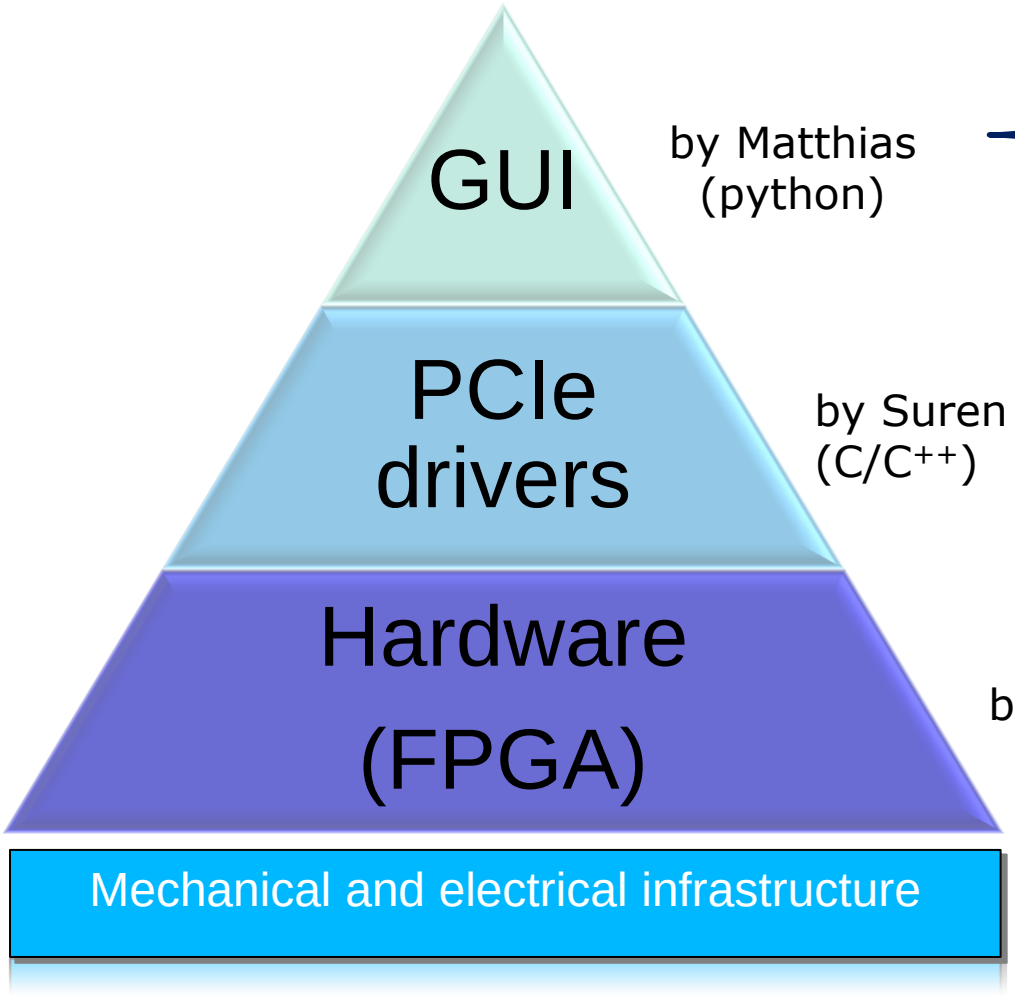
- Rows pedestal → less evident
- The vertical inefficiency columns → are not present
- Acquisition time (full frame) → 15 sec

FPGA architecture (diagram block)



- Design optimized for: high internal bandwidth =>2GB/s, smart design => 2% FPGA occupancy and lower FPGA power consumption
- 95 FSMs presents, several FPGA clock domains (48, 480 and 250 MHz)
- Status/errors and data consistency check → integrated
- Fully configurable camera → see Uros's talk

UFO HW & SW integration



by Matthias (python)

- Easy CMOSIS access for chip config.
- On-line camera temperature monitor
- On-line data display and analysis

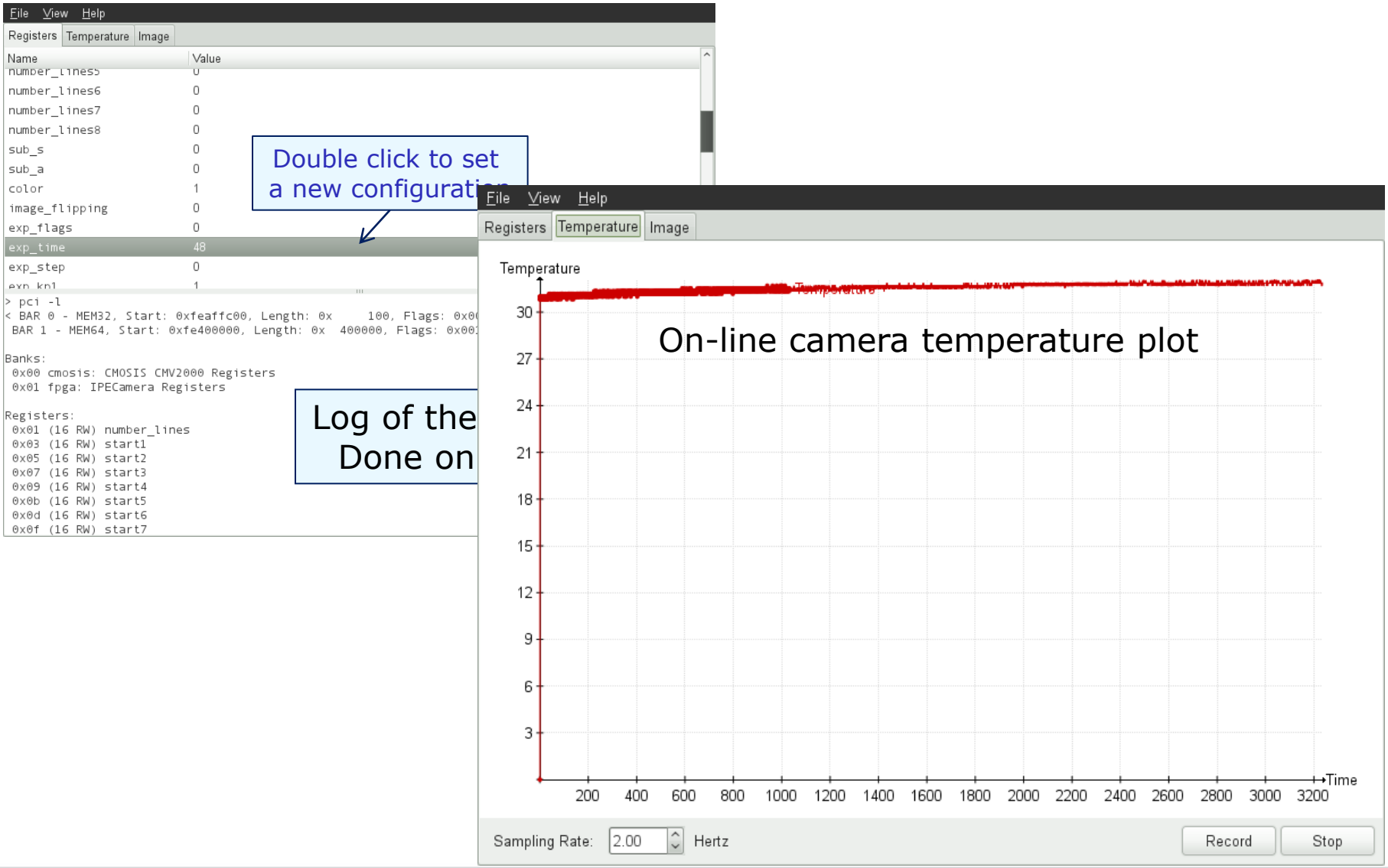
by Suren (C/C++)

- Full system control (Chip + FPGA)
- On-line data consistency check
- Off-line data display and analysis

by Uros and Michele (verilog)

by Armin

UFO - Graphic User Interface



What´s next

Hardware:

- DDR external RAM firmware integration → will allow to increase the speed @ 340 frame/sec
- DMA (10Gb/s) firmware integration

  → Both steps require an additional effort in the FPGA logic infrastructure
- HW implementation of a first prototype of the fast reject

Software:

- DMA requires a new dedicated driver that must be developed
- GUI must be re-adapted for new FPGA architecture

Detector side:

- As soon possible start with detector characterization in ANKA beam light laboratory → will start with PCO-edge

About the test Beam ?