

IPE camera Hardware & Software Status

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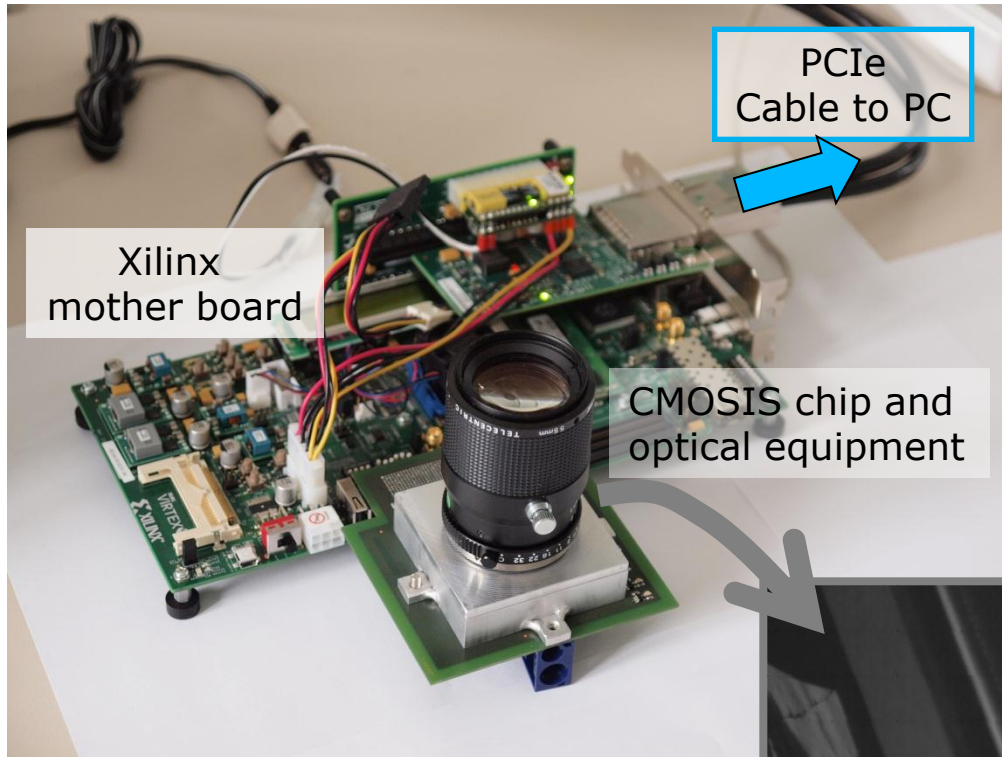


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Outline

- FPGA readout architecture → overview and status
 - HW and SW integration → overview and status
 - What's next
- see Uros's talk → IPE camera tuning and temperature control system

UFO Overview



In the last 3 months:

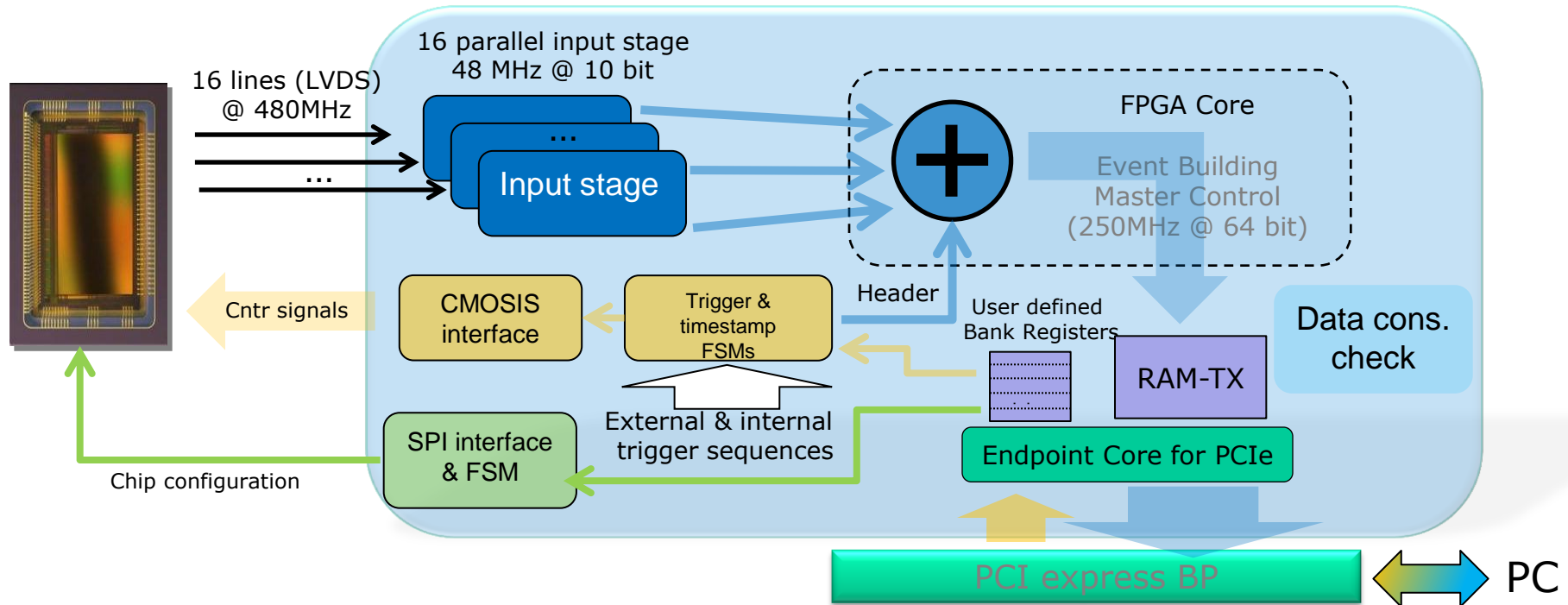
- HW – Firmware develop.
 - HW debug (mezzanine board)
 - Software develop. (driver+GUI)
 - Cooling system “proto” → details in Uros’s talk
 - Mechanical support
- Camera fully operational





- Rows pedestal → less evident
- The vertical inefficiency columns → are not present
- Acquisition time (full frame) → 15 sec



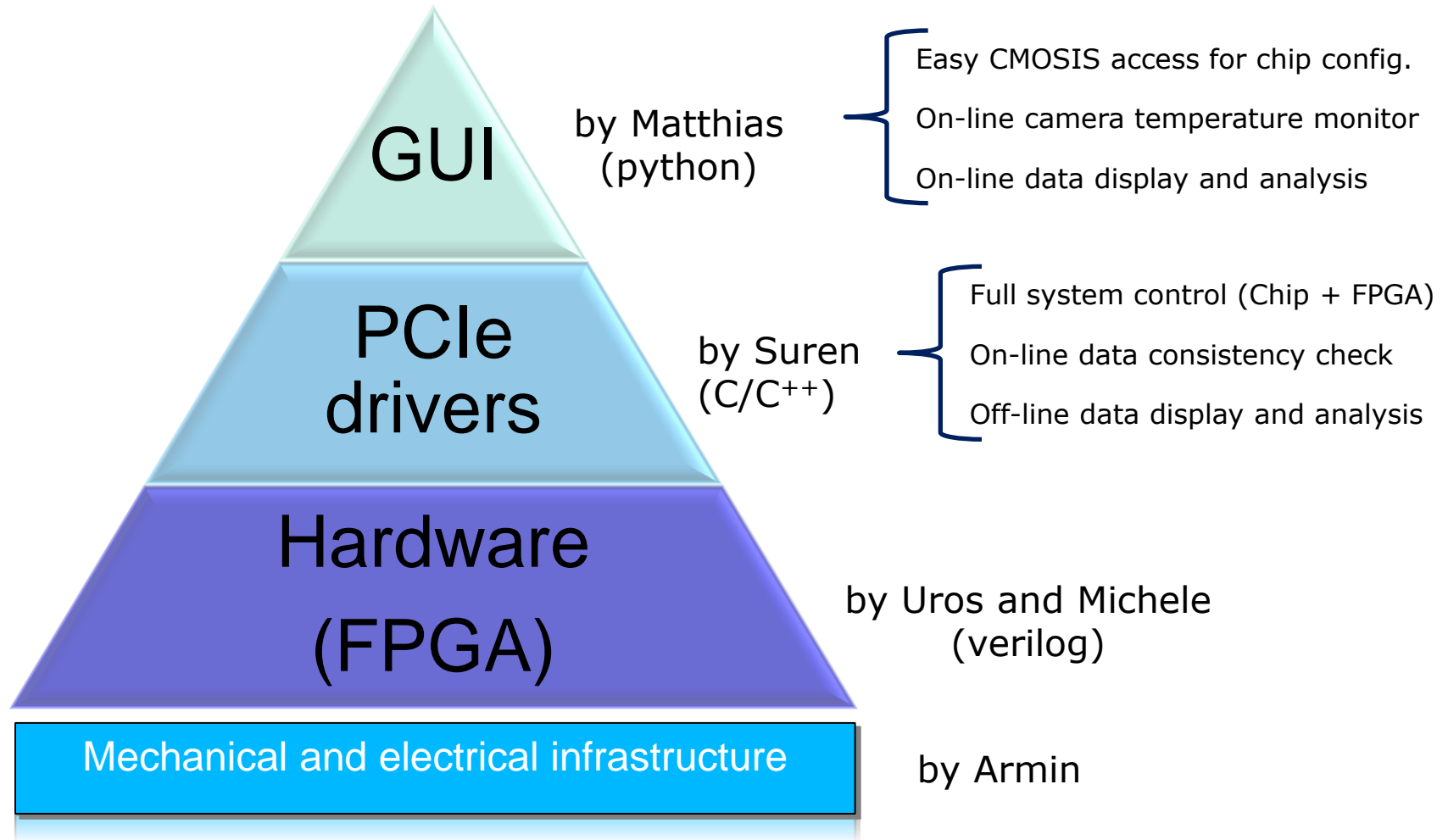
FPGA architecture (diagram block)

FPGA TOP

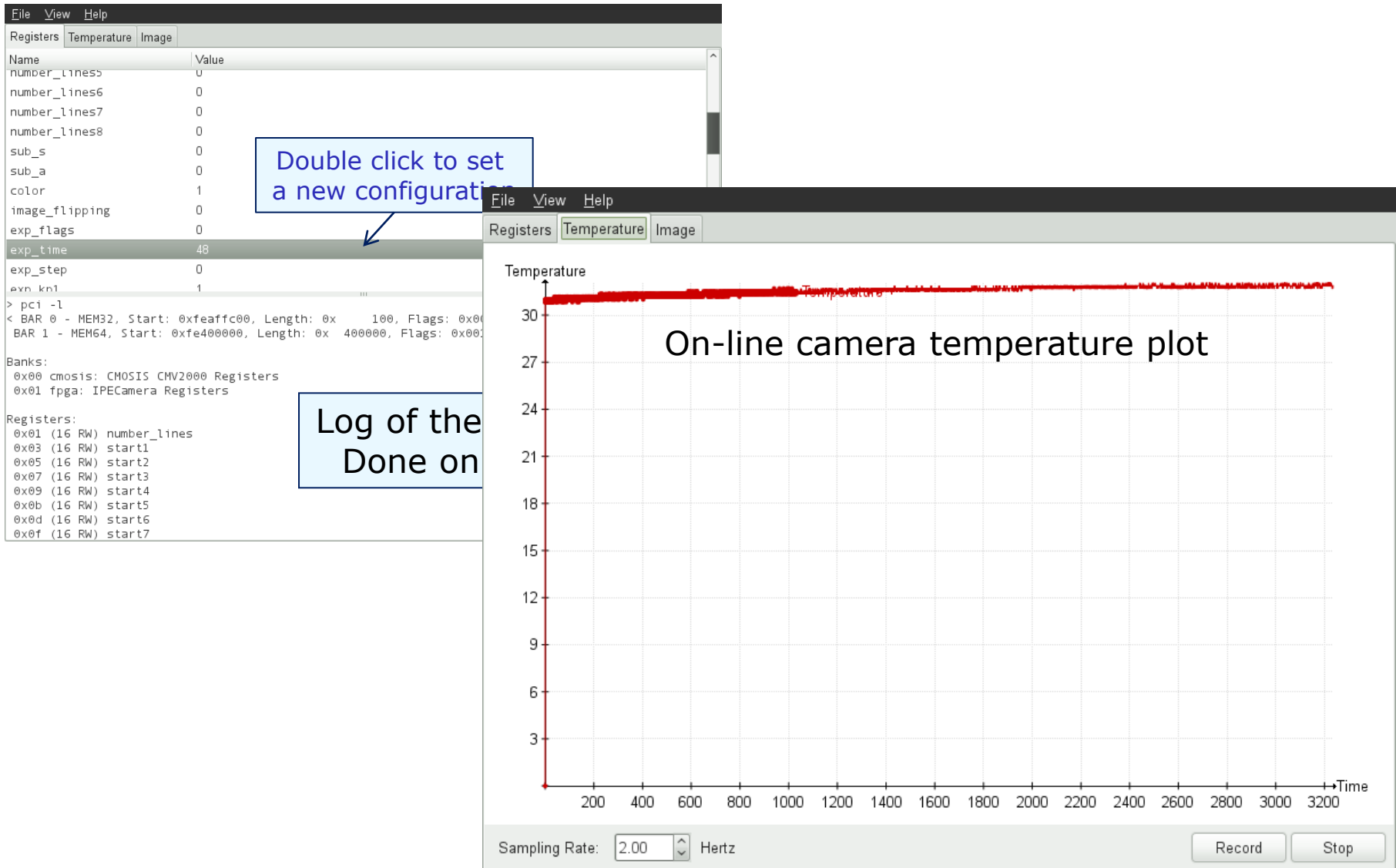


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 Design optimized for: high internal bandwidth =>2GB/s, smart design => 2% FPGA occupancy and lower FPGA power consumption
- 
 95 FSMs presents, several FPGA clock domains (48, 480 and 250 MHz)
- 
 Status/errors and data consistency check → integrated
- 
 Fully configurable camera → see Uros's talk

UFO HW & SW integration



UFO - Graphic User Interface



The screenshot displays the UFO GUI with two windows. The left window shows a 'Registers' table with various parameters and their values. A blue callout box points to the 'Registers' tab with the text 'Double click to set a new configuration'. The right window shows a 'Temperature' plot with a red line representing the temperature over time. A blue callout box points to the plot with the text 'Log of the Done on'. The plot has a y-axis labeled 'Temperature' ranging from 3 to 30 and an x-axis labeled 'Time' ranging from 0 to 3200. The temperature line is constant at approximately 31. Below the plot, there is a 'Sampling Rate' dropdown set to '2.00' Hertz, and 'Record' and 'Stop' buttons.

Name	Value
number_lines5	0
number_lines6	0
number_lines7	0
number_lines8	0
sub_s	0
sub_a	0
color	1
image_flipping	0
exp_flags	0
exp_time	48
exp_step	0
exp_kn1	1

Registers

```
> pci -l  
< BAR 0 - MEM32, Start: 0xfeaffc00, Length: 0x 100, Flags: 0x00  
BAR 1 - MEM64, Start: 0xfe400000, Length: 0x 400000, Flags: 0x00  
Banks:  
0x00 cmosis: CMOSIS CMV2000 Registers  
0x01 fpga: IPECamera Registers  
Registers:  
0x01 (16 RW) number_lines  
0x03 (16 RW) start1  
0x05 (16 RW) start2  
0x07 (16 RW) start3  
0x09 (16 RW) start4  
0x0b (16 RW) start5  
0x0d (16 RW) start6  
0x0f (16 RW) start7
```

Temperature

On-line camera temperature plot

Sampling Rate: 2.00 Hertz

Record Stop

What's next

Hardware:

- DDR external RAM firmware integration → will allow to increase the speed @ 340 frame/sec
- DMA (10Gb/s) firmware integration
→ Both steps require an additional effort in the FPGA logic infrastructure
- HW implementation of a first prototype of the fast reject

Software:

- DMA requires a new dedicated driver that must be developed
- GUI must be re-adapted for new FPGA architecture

Detector side:

- As soon possible start with detector characterization in ANKA beam light laboratory → will start with PCO-edge

About the test Beam ?