Karlsruhe Institute of Technology

# UFO
# Ultra fast X-ray imaging of scientific processes with on-line assessment and data-driven process control

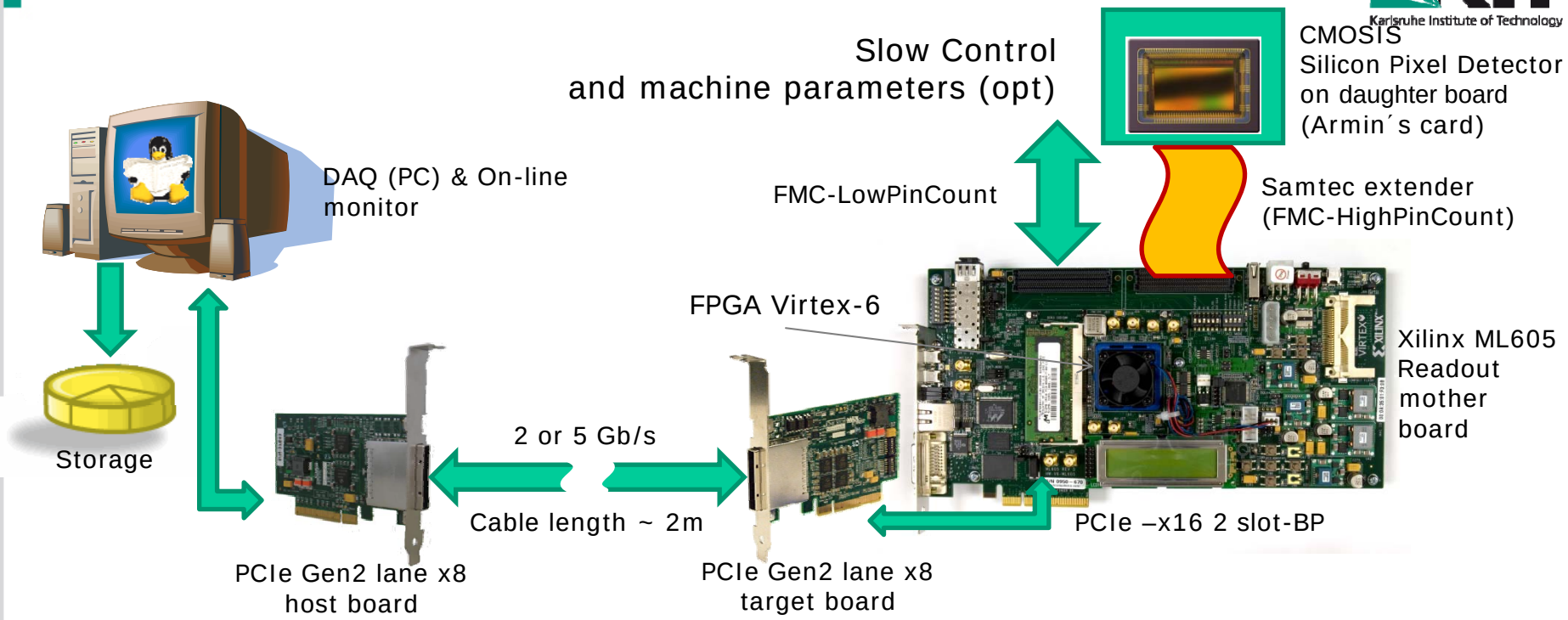
Forschungszentrum Karlsruhe in der Helmholtz-Gemeinschaft

Universität Karlsruhe (TH) Research University • founded 1825

## Outline

- Readout electronic & DAQ (Data AcQuisition) system → overview and status
- CMOSIS silicon pixel detector → some considerations
- Strategy to improve both ´fast reject algorithm´ and ´CMOSIS readout time´

# Readout & DAQ system - Overview



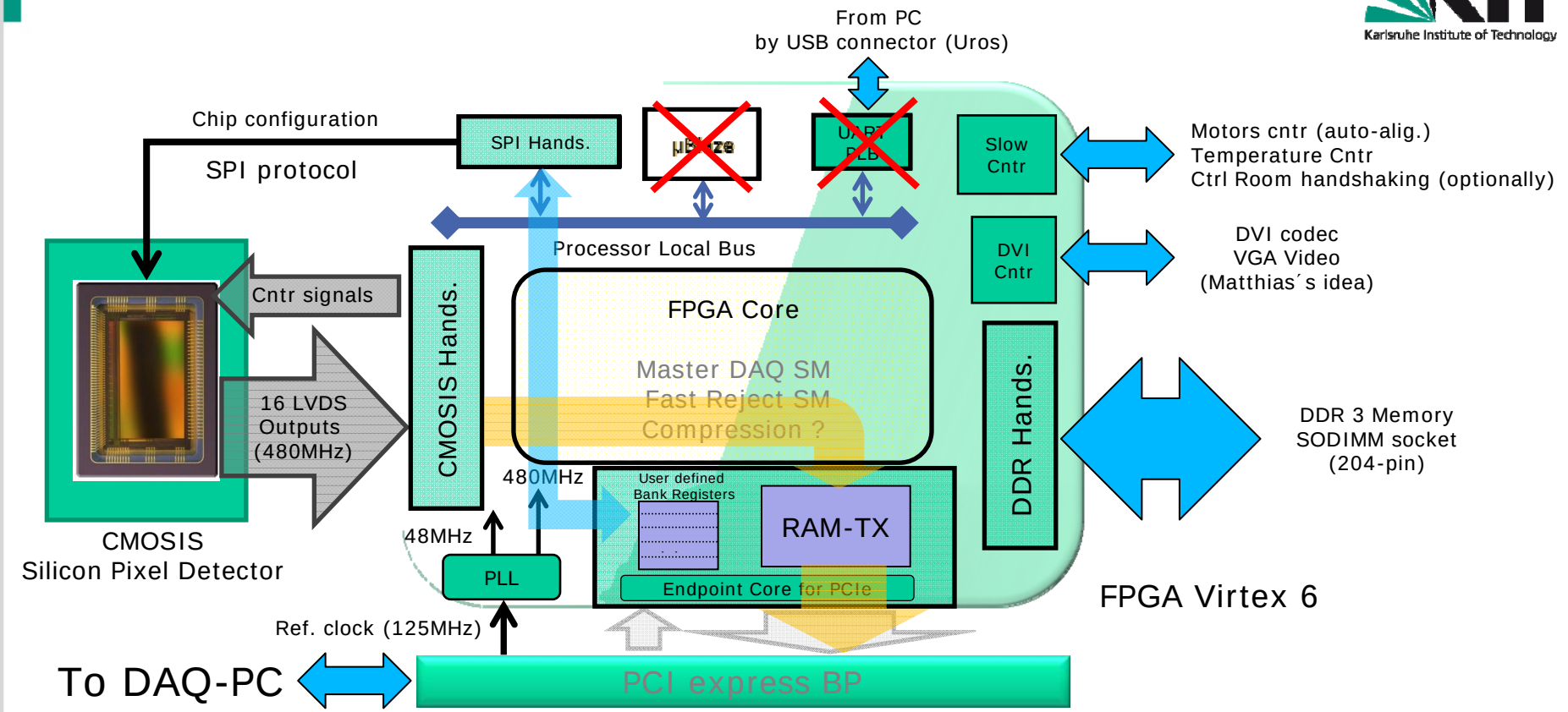

## Readout chain - Status

1. Chain is ready to be used
2. All in-board devices (DDR, FLASH mem, UART, etc. ) tested by Xilinx BIST (Built-In Self Test)

## What´s next

1. PCI endpoint module for communication between the mother board and PC by PCIe socket (Linux)
    1. Write/Read cycle @ different speeds → error bit rates
    2. Makes a internal connection between the SPI CMOSIS chip interface and PCI Bank Register
2. Design handshaking CMOSIS module and try to readout frames (Linux)

# FPGA internal architecture - TOP view




## Fpga firmware - Status

1. SPI Handshaking, µBlaze processor and UART interphase modules → generated by Uros
2. PCI top module (included Bank Register and RAM) → development actually under way (Matthias and Michele)

## What´s next

1. Connection between Bank Register and SPI Handshaking → to configure the CMOSIS directly by PCIe
2. CMOSIS Handshaking module and internal sequencer for free running frame acquisition (Michele)
3. DDR Handshaking and memory Cntr + Fast Reject algorithm modules (Michele and volunteer….)

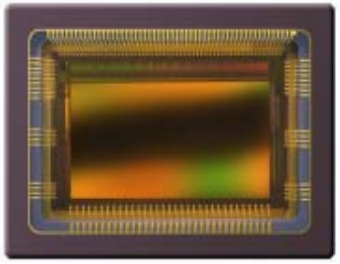
# CMV2000 Silicon Pixel Detector

Sensitive area consists in 2048x1088 pixels (5.5x5.5 $\mu m^2$), 5$\mu$m thick epi-layer

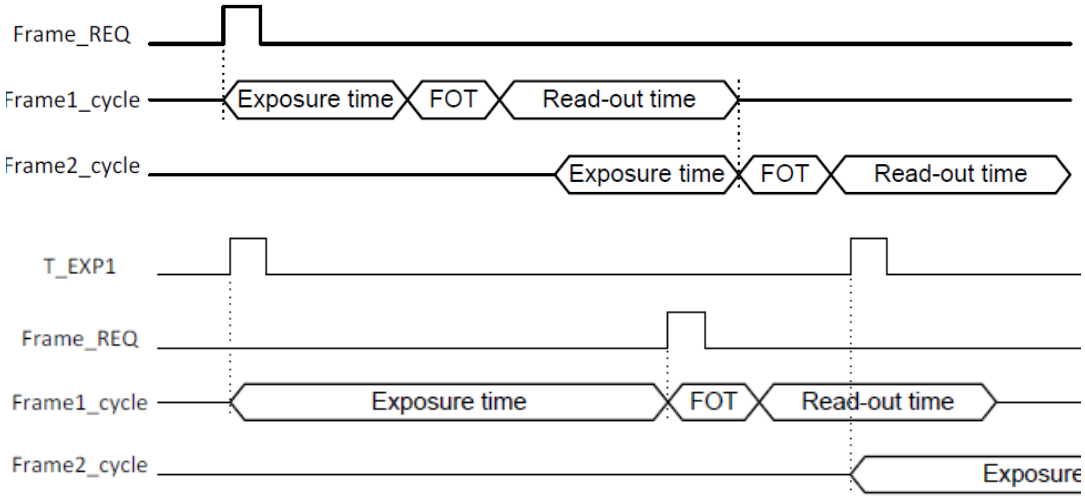
Column ADC converts the analog pixel value (energy released) → 10-12 bits

Reset noise (KT/C) cancelling through the Correlated Double Sampling

Fixed pattern noise is < 1LSB in 10 bit mode → with a SNR =60dB



## CMOSIS and FPGA handshaking for data taking




Internal exposure → the exposure time is set by programming the appropriate register by SPI interface.

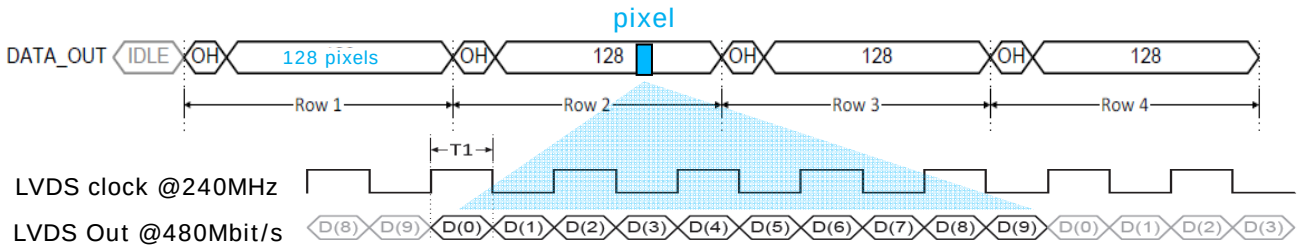
External exposure → exposure time is defined externally by T_EXP1 & Frame_REQ input pins

The `CMOSIS Interface module (FPGA)´ will generate both control signals and Frame_REQ & T_EXP1 for a flexible control of the exposure time.

**N.B** When the Readout chain will be available → As soon as the CMOSIS chip characterization could start → Offset (pixel threshold), gain, exposure time, Piecewise linear response, etc (Tomy´s suggestion)

# CMOSIS readout timing estimation

Column-wise organized Readout by 16 LVDS output channels, each LVDS reads out 128 adjacent columns @ 480 Mbit/s




## BW and max frame rate estimation for a full frame readout

$T_{pixel\_readout}$ = 10bits / 480MHz = 20.8ns/pix

$T_{ROW}$ = 20.8ns/pix * 128pix/row = 2.67µs/row

$T_{Frame}$ = 2.67µs/row * 1088rows ~ 2.9ms/frame

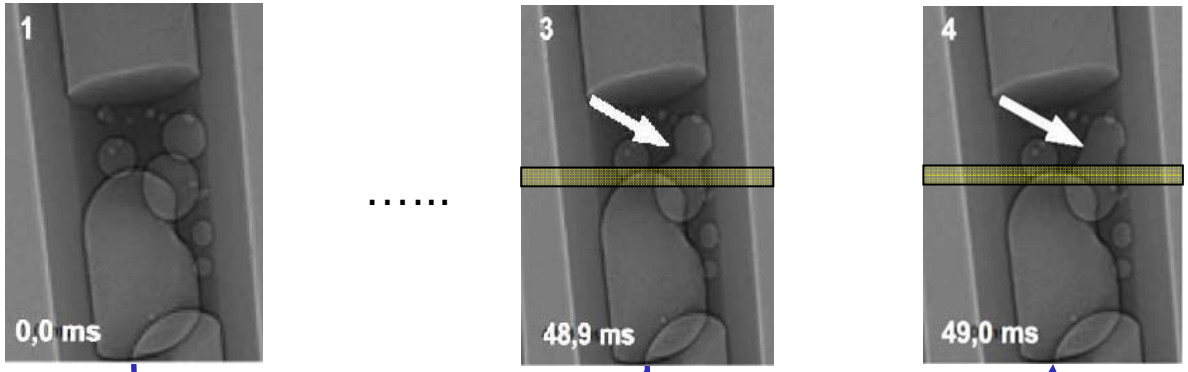
→ Frame rate ~ 340 frame/s

- The BW to transfer full readout frame at max frame speed → 20Mbit * 340 frame/s = 6.8Gbit/s → fast reject and data compression algorithms are necessaries to reduce the frame/s sent via PCIe to DAQ
- In any case the fast reject can not produce trigger signals more fast that 340 Hz
- A huge data sent from readout board represents a challenge for on-line reconstruction tools

→ How can we increase the frame rate and to reduce the amount of data coming from detector ?

# Subsampling interesting region strategy

BW estimation in a real case → both the temporal and spatial redundancies are considered

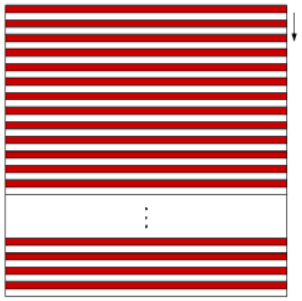



- Only 22 of 1088 rows are changed between `reference frame´ and ´Frame N´→ Total $Data_{Readout}$ = 450 kbit (all columns are read). → The total data sent to fast reject algorithm is drastically reduced
- The BW @ (assume a mean frequency value = 200Hz) = 450 * 200 = 90Mbit/s
  → BW remain factor 10 less that PCIe Bandwidth @ 2.5 Gbit/s → No additional data compression algorithm should be necessary
- The readout time → $T_{Frame}$ = 2.67 msec/row * 22 rows ~ 59 msec/frame → 17 kHz fr
  → The high speed fast reject signals (triggers) should be available

*How to do ?*

# Sub-sampling strategy for rows 'fast reject'

To maintain the same field of view but reduce the amount of data coming out of the detector, a subsampling mode is implemented on the chip → could be used to split a full frame in several distinct frames

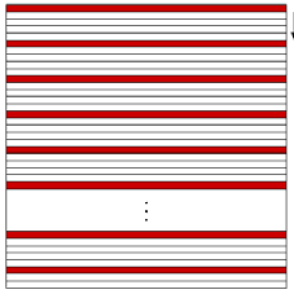


Full frame is split in two different frames:

$Frame_1$ → contain only the odd lines (white rows)
$Frame_2$ → contain only the even lines (red rows)

$T_{Frame}$ = 2.67 μsec/row * 544 rows ~ 1.45 msec/frame → about 700 frame/sec

For more frames



$T_{Frame}$ = 2.67 μsec/row * 109 rows ~ 291μsec/frame → about 3.4K frame/sec for 10 frames

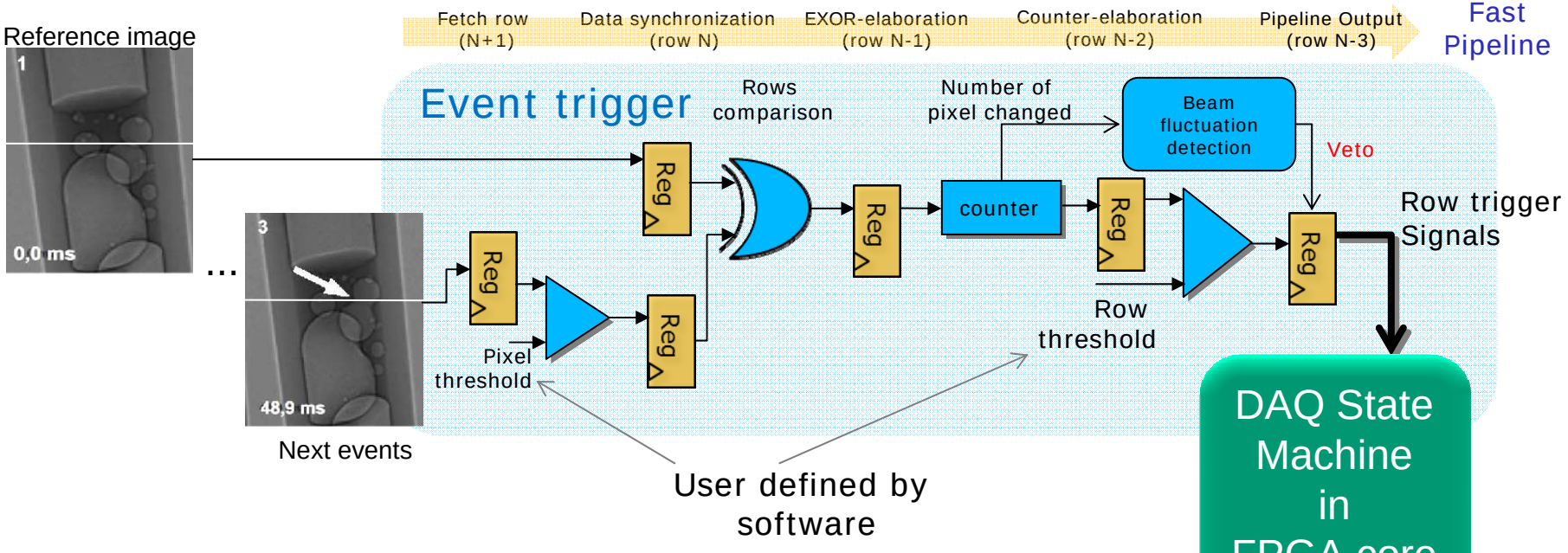
$T_{Frame}$ = 2.67 μsec/row * 54 rows ~ 145μsec/frame → about 7K frame/sec for 20 frames

The subsampling allows to design 'fast reject' algorithm operating @ kHz range and with a considerable reduction of data coming from the detector

# Sub-sampling strategy for rows 'fast reject'

Allows to generate fast reject signals (triggers) @ rows level → starting from a reference image

Subsampling strategy is used to allow a fast readout frame @ kHz range

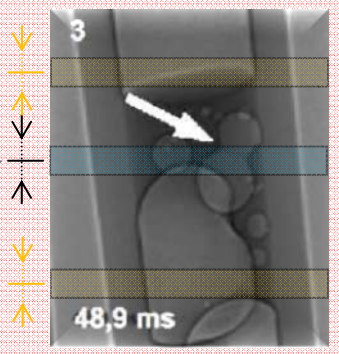



## Event Readout

To limit the amount of data and increase the frame rate from sensor, windowing in Y direction is possible. The number of lines and start address can be set by SPI

Readout of a window around the row trigger signal or full frame can be requested

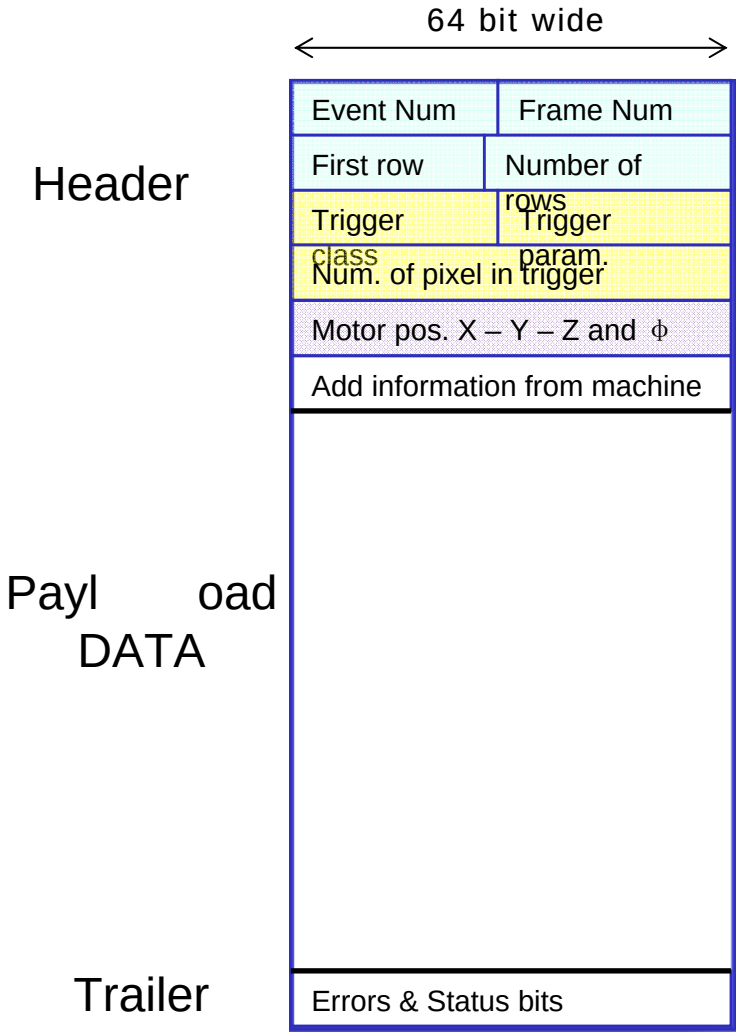
Optionally the multiple windows can be defined when a multiple rows trigger are presents




SPI chip configuration signals

# Preliminary data format proposal

The data stream coming from detector will be re-formatted before to be sent to on-line PC.




Header data used for both consistency frame check and on-line reconstruction → Andreas and Michele

→ Event identification and reconstruction

→ Trigger class → which algorithm is set for caching trigger events and which programmable parameters

→ Motor position could be play a rule on the reconstruction

→ Additional information coming from the machine control room (Optionally)

Data coming from CMOSIS silicon detector

Trailer used as End-Of-Packet

# Conclusions & what´s next

## Conclusion

- The readout chain → tested and ready for data taking
- One ´Fast Reject` and `Readout´ strategies have been defined → using both ´sub-sampling´ and ´Windowing´ built-in CMOSIS chip features

  (Reference on CMOSIS datasheet pag. 26 – 29)

## What´s next

- SPI chip configuration by PCIe → must be developed
- ´CMOSIS readout module` → must be developed

- When the first readout chain is available, the CMOSIS chip characterization will start using a light source